PHASE LOCKED LOOP BEHAVIORAL MODELING

Elena Doicaru, Gheorghe Grama

University of Craiova, Faculty of Automation, Computer Science and Electronics
Bvd. Decebal, Nr.5, 1100 Craiova, ROMANIA, e-mail: dmilena@electronics.ucv.ro

The Institute for the System Analyses (INAS-SA), Str. Caracal, Nr. 244,
Craiova,ROMANIA, e-mail:ggrama@inas.ro

Abstract: In this paper are presented the simulation possibilities of complex systems as phase locked loop (PLL) integrated circuits and an analog behavioral macro model for the standard PLL integrated circuit LM565. Using this behavioral macro model, were simulated several typical applications of PLL as FM demodulator, FSK demodulator and frequency multiplier; the results of simulations are also presented.

Keywords: simulations, behavioural modelling, PSPICE, PLL.

1. INTRODUCTION

In the analog computer aided design, the simulation becomes a standard approach in the optimization and in the validation of circuit performances. The accuracy and the representatively of the results depend on the primitive models available in the simulation packages and on the technological parameters given by the IC manufacturers. The main problem, which must be solved in the simulation of complex systems, is the conflict between the accuracy and the simulation time. It is known the fact that when the number of transistors becomes significant the simulation time becomes prohibitive and the convergence problems can appear. But, it is known also the fact that when we pass to a higher hierarchical description level of a circuit, the information loose increases and the simulation time decreases. Also, it must remark that the device models used in SPICE programs, develop for the standard IC technologies, are not suitable for the modern technologies used in realizing these device (for example the submicron MOS transistors) and thus they give considerable errors. The accuracy of these models can be improved by using so called structural macro modeling method. The structural macro modeling method consists in building new models for devices by using the existing SPICE intrinsic models completed with proper elements. But, this method can not be used for complex circuits.

For the simulation of the complex circuits exists three methods that give a good solve of the conflict accuracy-simulation time.

- The first method is *the C code modeling*. This consists in creating a C code subroutines that describes the static and dynamic equations of the circuits. It is also used for improve the accuracy of device models. The greatest advantage of this type of modeling is the flexibility (all types of nonlinear algebraic and differential equations can be modeled in this way). The most significant disadvantages of this method are: the nonexistence of a universal accepted C code (thus the developed models can be moved without problems from one simulator to another) and the difficulty to investigate and solve the convergence and stability problems of the simulation.
- The second method is the *AHDL (Analog Hardware Description Language) modeling*. This method is especially used to develop new models for the mixed integrated circuits and for analog circuits implemented in new technologies. Unfortunately the SPICE simulators can't use the so implemented models.
- The third method is so called *Analog Behavioral Macromodeling (ABM)*. This new and

powerful modeling technique is building models for devices, subcircuits and complex circuits using the nonlinear controlled voltage and current sources to implement the static and dynamic equations which proper characterize the functional behavioral of these. The greatest advantages of the ABM method are the portability to all the modern SPICE simulators and also the easy access to the model internal equations and parameters. More, despite of differences of syntax between differnt types of SPICE, the translation between them needs minimal syntax adjustments.

2. THE PSPICE ABM

In this section is briefly presented the PSPICE ABM feature. The ABM consists in flexible description of electronic devices and circuits in terms of a transfer function or lookup table. In other words, a mathematical relationship is used to model a circuit segment so the segment need not be designed component by component.

The symbol library file (abm.sbl) contains several ABM parts that can be classified as either control system parts or as PSPICE A/D-equivalent parts. Control systems parts are defined with the reference voltage preset to ground so that each controlling input and output are represented by a single pin in the symbol. The PSPICE A/D-equivalent parts reflect the structure of the E and G device types which respond to a differential input and have double-ended output.

The control system parts can be grouped by function:

- The basic components provide fundamental functions: CONST, SUM, MULT, GAIN, DIFF;
- The limiters can be used to restrict an output to values between a set of specified ranges: LIMIT, GLIMIT, SOFTLIM;
- The Chebyshev filters: LOPASS, HIPASS, BANDPASS, BANDREJ;
- The integrator and the differentiator: INTEG, DIFFER;
- The table look-ups provide a lookup table that is used to correlate an input and an output based on a set of data points: TABLE, FTABLE;
- The Laplace transform (LAPLACE);
- The math functions: ABS, SQRT, PWR, PWRS, LOG, LOG10, EXP, SIN, COS, TAN, ATAN, ARCTAN;
- The expressions functions: ABM, ABM1, ABM2, ABM3, ABM/1, ABM1/1, ABM2/1, ABM3/1; each of these parts has a set of four expressions and can have one, two or three inputs and one voltage or current output.

The PSPICE A/D-equivalent parts available in the symbol library can be also grouped by function:

- The mathematical expressions: EVALUE, GVALUE, ESUM, GSUM, EMULT, GMULT; these components always have the voltage inputs and the controlled outputs can be either voltages (E types) or currents (G types);
- The look-up tables use a transfer function described by a table: ETABLE, GTABLE; these components are suitable for use with measured data;
- The frequency look-up tables are described by a table of frequency response in either the magnitude/phase domain or complex number domain: EFREQ, GFREQ;
- The Laplace transforms allow a transfer function to be described by a Laplace transform function: ELAPLACE, GLAPLACE.

The ABM method assures a comparable accuracy with C code and AHDL modeling techniques, and also assures a simple and easier modeling procedure. It must be pointed that the ABM macro models are not compiled models and thus the simulator at each analysis time step interprets them. That brings a slightly increase of the simulation time comparatively with the two above mentioned modeling techniques.

3. THE PLL MODELING

Simulating the operation of PLLs is nontrivial because of the very wide range of time constants present in PLLs. So, it is known that, the standard PLL integrated circuits contain a Schmitt trigger for the voltage-controlled oscillator (VCO), a Gilbert multiplier for the phase detector and the first (or second) order low-pass filter is external added. Typically, the VCO has nodes with important time constants much smaller than the period of its output waveform. More, the time constant of low-pass filter are order of magnitude greater than the VCO's period.

The simulation with SPICE of this circuit at the transistor level is very difficult and not sure because:

- the topology is too complex;
- the IC internal elements are not all available;
- the time steps must be less than the smallest time constant of the VCO, whereas the total simulation time must be greater than the largest time constant of the low-pass filter.

Even if it is known the IC internal elements, the simulation time for this is exorbitant and this kind of simulation is usually impractical.

The solution for simulation of these kinds of circuits is based on the simplified models in which the continuous time components are replaced by approximately equivalent difference-equation models. So we say, this approach can be done by using difference-equations simulator, such us the Simulink program in Matlab and ABM in PSPICE or by writing custom difference-equation simulations using the C code. The advantages and disadvantages of these methods have been presented in the first section.

With ABM technique the PLL integrated circuits can be modeled by using a cascade of a multiplier function, a first (or second) order low-pass filter and a VCO, so that the fundamental equations that

describe the function of the circuit to be implemented.

The fundamental equations are:

- for the comparison between frequency
  - the multiplication

$$\begin{aligned} v_{0m}(t) &= K \cdot s_i \cdot s_{osc} \\ s_i &= V_i \cdot \sin(\omega_i \cdot t) \\ s_{osc} &= V_{osc} \cdot \sin(\omega_{osc} \cdot t + \theta) \end{aligned} \quad (1)$$

  - the low-pass filtering

$$\begin{aligned} v_0(t) &= \int_{-\infty}^{t} v_{0m}(\tau) \cdot f(t-\tau) \cdot d\tau \cong \\ &\cong K_D \cdot \sin\left(\frac{\pi}{2} - \theta\right) \end{aligned} \quad (2)$$

  where $f(t)$ is the indicial response of filter and

$$K_D = K \cdot V_i \cdot V_{osc} \cdot F_0 \quad (3)$$

  is a constant, called phase detector sensitivity, that depends of the input signal amplitude, output VCO amplitude, scale coefficient of multiplier K and static gain of low-pass filter (for frequency $f = 0$) F_0.

  The Laplace domain transfer function of filter is:

$$F(s) = \frac{F_0}{1 + \tau_1 \cdot s}, \quad (4)$$

  or

$$F(s) = \frac{F_0 \cdot (1 + \tau_2 \cdot s)}{1 + (\tau_1 + \tau_2) \cdot s} \quad (5)$$

  for the first order filter (lag or lead-lag respectively), and

$$F(s) = \frac{F_0 \cdot \omega_0^2}{\omega_0^2 + 2 \cdot \omega_0 \cdot s + s^2} \quad (6)$$

  for the second order filter.

- for the output frequency generation with VCO

  The PLL is a highly nonlinear system. Fortunately, once a PLL circuit is in lock, its dynamic response to input signal-phase and frequency changes can be well approximated by a linear model, as long as these changes are slow and small about their operating or bias point. So, the total phase at any instance in time is given by:

$$\Phi_{osc}(t) = \omega_{osc}(t) \cdot t + \theta_{osc}(t) \quad (7)$$

  where $\omega_{osc}(t)$ and $\theta_{osc}(t)$ are both deterministic signals that slowly change with time.

  The instantaneous frequency is defined to be:

$$\omega_{osc\,inst}(t) = \frac{d\Phi_{osc}(t)}{dt} = \omega_0 + K_0 \cdot v_0(t) \quad (8)$$

  where K_0 is a constant relating the change in instantaneous frequency to control voltage ratio and called VCO sensitivity and $f_0 = \omega_0 / (2 \cdot \pi)$ is called the VCO free running frequency.

  By integrating the (5) relation we obtain:

$$\begin{aligned} \Phi_{osc}(t) &= \omega_{osc}(t) \cdot t + \theta_{osc}(t) = \\ &= \Phi_{osc}(0) + \int_0^t \omega_{osc\,inst}(\tau) \cdot d\tau = \\ &= \omega_0 \cdot t + K_0 \cdot \int_0^t v_0(\tau) \cdot d\tau + \Phi_{osc}(0) \end{aligned} \quad (9)$$

  and we can conclude that the instantaneous phase is the integral of the instantaneous frequency.

So, the multiplier function (1) can be implemented by:

- an EVALUE component (voltage controlled voltage source) followed by the limiter component:

`E_`*<name>* `$N_`*<connecting nodes>* `VALUE { V($N_+`*node*`, 0)*V($N_-`*node*`, 0)*`K_D`}`

`E_`*<name>* `$N_`*<connecting nodes>* `VALUE {LIMIT(V($N_+`*node*`),`*lower limit value*`,`*upper limit value*`)}`

- an ETABLE component (voltage controlled voltage source, that permits the piece-wise-linear approximation of the input-output transfer function) with the output range constrained to convenient limits:

E_<*name*> $N_<*connecting nodes*> TABLE {
K_D*V($N_+*node*, 0)*V($N_-*node*,0) }
+ ((*lower limit input value*, *lower limit output value*)
(*upper limit input value*, *upper limit output value*))

The low-pass filtering function (2) can be implemented by an ELAPACE component (voltage controlled voltage source, that enable the simulation of the Laplace transfer function) using the Laplace domain transfer function (4) or (5) or (6):

`E_E2 $N_<` *connecting nodes* `> LAPLACE { V($N_+`*node*`, 0) } = { 1/(1+`τ_1`*s) }`

The output frequency generation function (9) can be implemented by a GVALUE (voltage controlled current source) component with a capacitor load for the integral term of this relation, followed by an EVALUE component for obtaining the sinusoidal function $\sin\Phi_{osc}(t)$:

`G_G1 $N_<` *connecting nodes* `> VALUE { V($N_+`*node*`, 0)*0.000001*`K_0 `}`
`C_C1 $N_<` *connecting nodes* `> 1u`
`R_R4 $N_<` *connecting nodes* `> 1g`
`E_E3 $N_<` *connecting nodes* `> VALUE {`
`sin(6.28*`f_0`*(time+(1/(6.28*`f_0`))*V(0, $N_+`*node*`)))}`

In figure 1 is given the PLL generic behavioral modeling described before. The phase detector has K_D like parameter, the first order low-pass filter has the parameter tau1 and the VCO has parameters f_0 and K_0. The resistor R_4 is used for convergence reasons. The values of f_0, K_D and K_0 parameters are typical for LM565, but we can see that easily these it can be changed.

In this paper, using MicroSim PSpice A/D simulator, we develop a more elaborated behavioral model for the standard PLL integrated circuit produced by National Semiconductor Corporation, LM565.

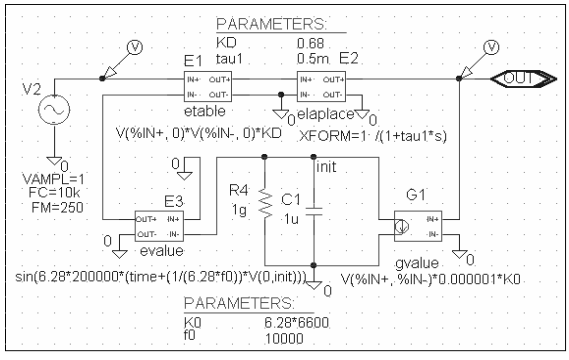

Figure 1. The PLL generic behavioral modeling.

By development of this model we have tried to solve the following aspects:

- the real topology of circuit;
- the real voltage level of circuit pins;
- the variation with VCO free-running frequency of PLL parameters: oscillator sensitivity, the lock bandwidth;
- the variation with supply voltage of following parameters: oscillator sensitivity and lock bandwidth.

The structural architecture with connection diagram is shown in figure 2. It can see that the VCO free-running frequency is determinated by external components C_0 and R_0. Also, the low-pass loop filter must be connected to the integrated circuit. In concordance with manufacturer indications, a simple lag filter or a lag-lead filter may by used. These kind of filters are forming from internal resistance at pin 7 (with value $3{,}6\text{K}\Omega$) and suitable external components.

According with the data sheet, the circuit performances in close loop are given by the following relationships:

$$f_0 = \frac{0.27}{R_0 \cdot C_0} \tag{10}$$

$$K_0 = \frac{54 \cdot f_0}{V_{a\lim}} \tag{11}$$

$$K_D = 0{,}68\ V/rad \tag{12}$$

$$B_U = \frac{16 \cdot f_0}{V_{a\lim}} \tag{13}$$

$$B_C = 2 \cdot \sqrt{2} \cdot f_n$$

$$f_n = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{K_0 \cdot K_D}{\tau_1}} \quad \text{for simple lag filter} \tag{14}$$

$$f_n = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{K_0 \cdot K_D}{\tau_1 + \tau_2}} \quad \text{for lag - leag filter}$$

$$V_{REF} = \frac{12{,}15\text{K}\Omega \cdot V^+_{\text{alim}} + 1{,}75\text{K}\Omega \cdot \left(V^-_{\text{alim}} + V_{BE}\right)}{13{,}85\text{K}\Omega} = 0.126354 \cdot \left(V^-_{\text{alim}} + V_{BE}\right) + 0{,}877256 \cdot V^+_{\text{alim}} \tag{15}$$

In figure 3 is shown the developed behavioral model of the PLL integrated circuit LM565. It is shown also the created SPICE symbol. The functional terminals of symbol correspond with the pins of LM565 package. The SPICE netlist of developed model is:

```
.SUBCKT LM565-X 1 2 3 4 5 6 7 8 9 10
C_C1 0 init 1u
R_R3 $N_0001 6  1.75k
R_R4 0 init 1g
R_R6 8 9 10g
R_R2 3 0 10g
R_R1 $N_0002 7 3.6k
E_E15 $N_0002 0 VALUE { V($N_0003, 0)+V(6,0) }
E_E1 $N_0003 0 TABLE { 0.68*V(2, 0)*V(5,0) }
+ ( (-0.68,-0.68) (0.68,0.68) )
G_G1 init 0 VALUE { (V(7,
+ 0)-V(6,0))*0.00001458/(R0*C0*(V(10,0)-V(1,0))) }
E_E13 4 0 VALUE
{sin(6.28*(0.27/(R0*C0))*(time+(R0*C0/(6.28*0.27))
*V(0,init))) }
E_E3 $N_0001 0 VALUE
{0.126354*(0.7+V(1,0))+0.873646*V(10,0) }
.ENDS
```

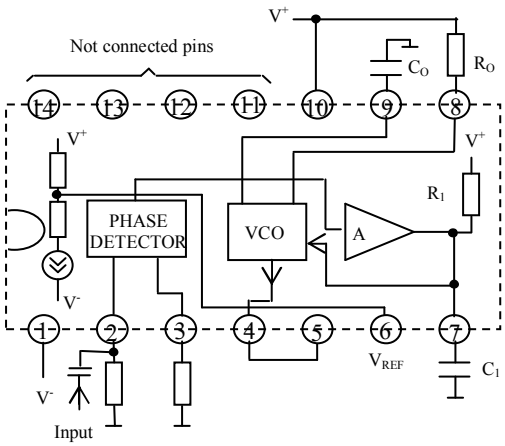

Figure 2. The structural architecture with connection diagram of LM565

A transient analysis is run to analyze the capture and lock ranges. The PLL input is attacked by a signal those frequency firstly rises from a lower value (lower than $f_0 - B_C/2$) at a value greater than $f_0 + B_U/2$, and secondly diminishes from a value greater than $f_0 + B_C/2$ to a value lower than $f_0 - B_U/2$. The schema used for simulation with the simulation results is shown in figure 4. It can see that the PLL does not respond to the input signal until the input signal frequency reaches the lower capture range frequency. Once lock is attained, the output voltage of PLL tracks frequency changes of the input signal and orders changes to the VCO frequency. But, when the input frequency exceeds the upper lock range frequency the PLL output voltage suddenly drops. Similarly, at the diminishing of frequency the PLL output does not respond until the input signal frequency reaches the upper capture range frequency and, once lock is attained, the PLL output voltage changes VCO frequency. When the lower lock range reaches, the PLL output voltage also suddenly drops. It can see also that for the chosen VCO free-running frequency and supply voltage, the values of capture and lock ranges respect the relations (13) and (14). The simulation time of these analyses, for a step ceiling of 25us and a print step of 25us, was around 8s.

We use this behavioral model of LM656 integrated circuit to simulate some typical applications given in his data sheet. Firstly, we simulate the FM demodulator application. The schema used for simulation and the simulation result are presented in figure 5. The simulation time, for a step ceiling of 2.5us and a print step of 2.5us, was around 4s. Next, we simulated a FSK demodulator, presented with the simulation result and input stimulus in figure 6. For this application, the simulation time, for a step ceiling of 25us and a print step of 25us, was around 15s. The last simulated application was a frequency multiplier.

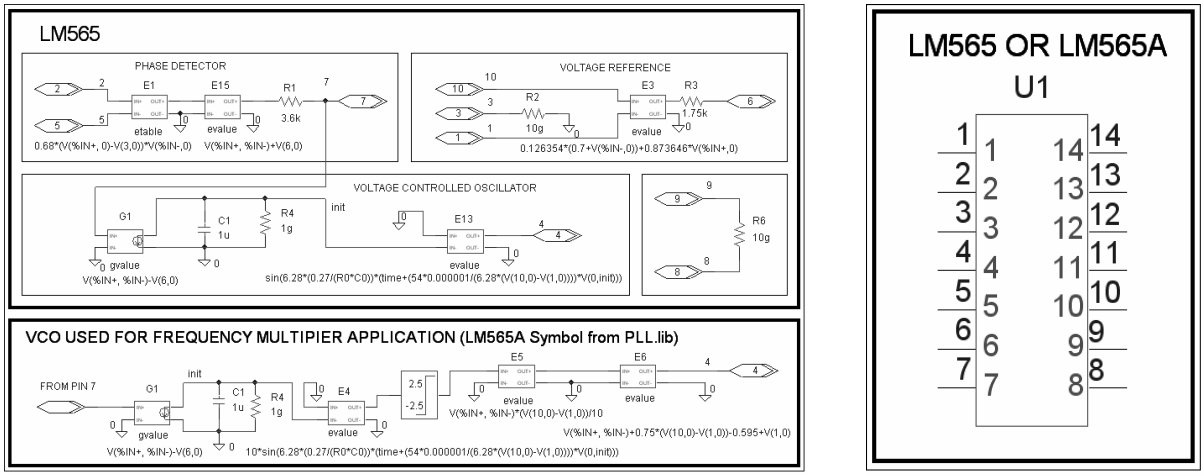

Figure 3. The developed behavioral model of the PLL integrated circuit LM565.

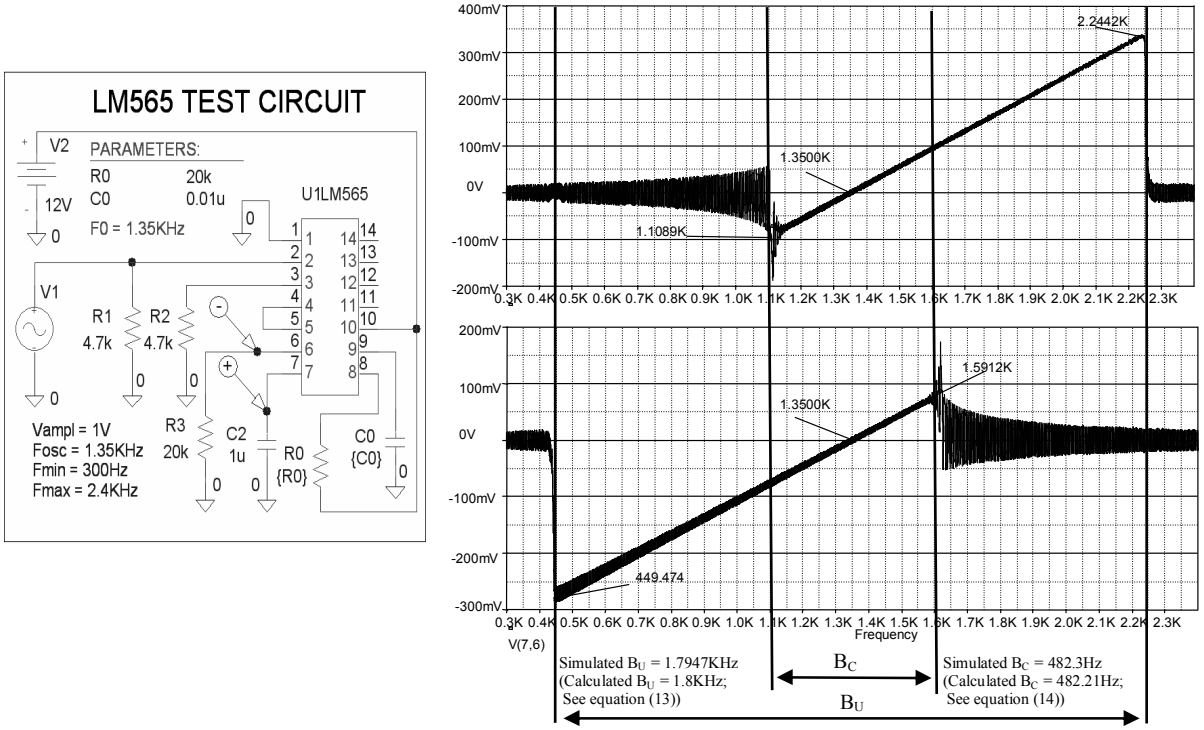

Figure 4. The schema used for the transient analysis to relieve the lock and capture ranges and the simulation results.

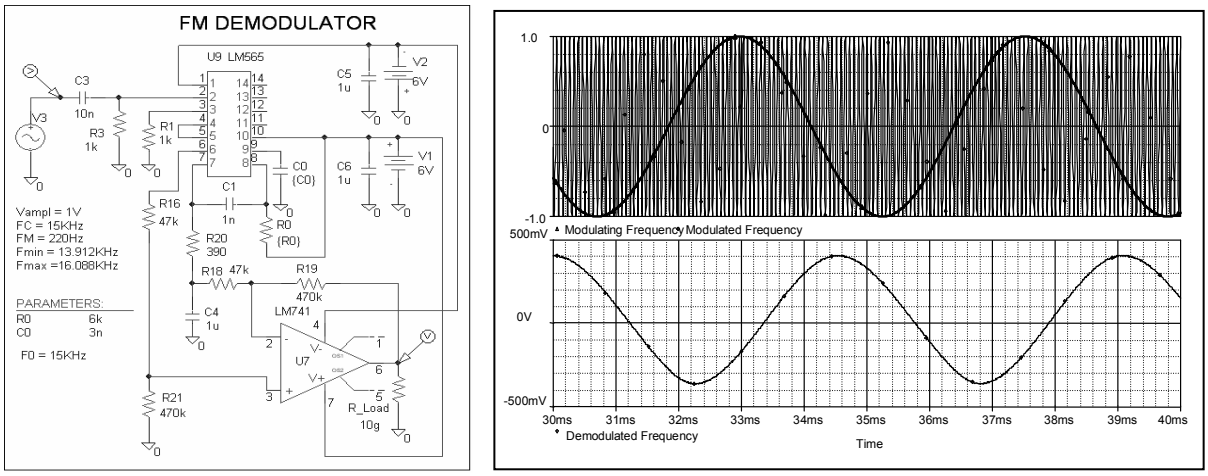

Figure 5. The schema used for simulate the FM demodulator application and the results of simulations.

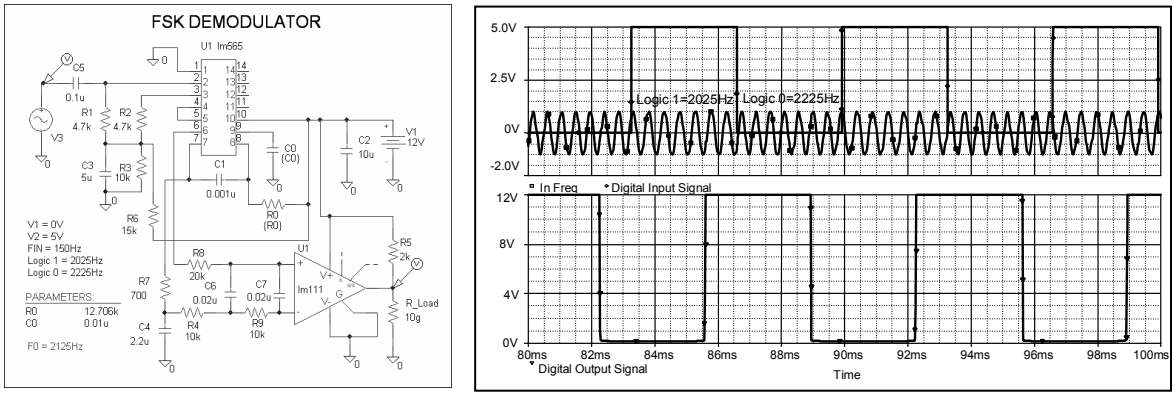

Figure 6. The schema used for simulation of FSK demodulator application and the simulation results.

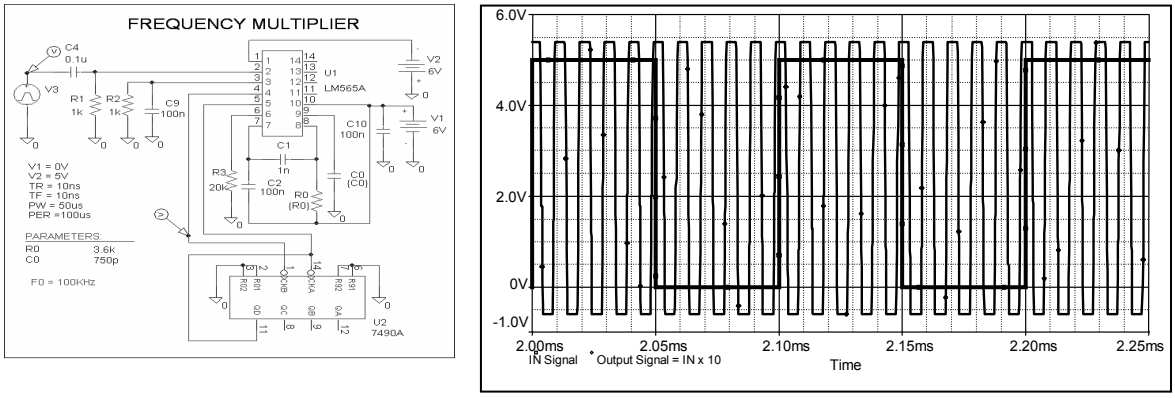

Figure 7. The schema used for simulation of frequency multiplier application and the simulation results.

For this application, the initial behavioral model of LM565 was modified (see figure 2) so that the real wave form and voltage level at VCO output to be respected. The simulation schema and simulation result are shown in figure 7. The simulation time, for a step ceiling of 0.25us and a print step of 0.25us, was around 8s.

3. CONCLUSION

In this paper firstly have been presented the conceptual techniques suitable for complex systems simulations and it is shown what are the advantages and the inconveniences of each one. Next we develop a PSPICE behavioral generic model and then a more elaborate PSPICE behavioral model for the LM565 PLL integrated circuit. This model respects the real topology and voltage levels at package pins of LM565. More, the model includes the influence of voltage supply and VCO free-running frequency of the PLL functional parameters. We run several transient analyses that demonstrate the model accuracy and give information about simulation time. We created a PLL library for general use. We wish to complete this library with others PLL circuit behavioral models (especially PLL with charge-pump and exclusive-OR phase comparators). Finally, we had run the transient analysis of several typical applications to check the developed models. All analysis point out that the simulation time is not prohibitive and that our model offers a good compromise accuracy - simulation time.

REFERENCES

Analogy Inc. (1990). *Saber User's Guide.* Release 3.0. Beaverton.

Andreu, D., D. Stepan and S. Josse, (2001). Introduction to behavioral modeling. Phase loop locked behavioral modeling. *Newsletter www.spice-club.com.*

Boucher, J., H. Schneider (1999). Design and Realization of Analog Simulator for Real Time Estimation of an Electrotechnical System State, *Newsletter,* Microelectronic Laboratory of National Polytechnic Institute ENSEEIHT – INP, Toulouse.

Johns, A. D. and K. Martin 1997. Phase locked loop. *Analog integrated circuit design*, **Volume no II**, page 648-695, Published by john Wiley & Sons, Inc., Toronto.

Lee, T. H. (1998). Phase locked loop. *The Design of CMOS Radio-Frequency Integrated Circuits*, page 438-483, Cambridge University Press.

Microsim Corporation. (1991). *PSPICE, Circuit Analysis User's Guide*, *Version 5.0.*

National Semiconductor Corporation (1995). *Data Book.*

Sedra, A. and K. C. Smith (1991). *Microelecronic Circuits*. Holt, Rinehart &Winston/Sounders, 3rd edition, New York.

Vladimirescu, A. (1999). *SPICE, Editura Tehnica, Bucuresti.*

Microsim Corporation. (1991). *PSPICE, Circuit Analysis User's Guide*, *Version 5.0.*