PERFORMANT CMOS ACTIVE RESISTOR BASED ON IMPROVED LINEARITY DIFFERENTIAL STRUCTURES

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Abstract: An original active resistor circuit will be presented, having the main advantages of an improved linearity, a small area consumption and a very good frequency response. An original technique for linearizing the $I(V)$ characteristic of the active resistor will be proposed, based on the utilization of a new linear differential amplifier and on a current-pass circuit. The linearization of the original differential structure will be achieved by implementing an original method of compensating the quadratic characteristic of the MOS transistor working in saturation by two complementary square-root circuits. The errors introduced by the second-order effects will be quantitative evaluated, while the circuit frequency response of the circuit will be very good as a result of biasing all MOS transistors in the saturation region and of a current-mode operation of the square-root circuits. The active resistor is implemented in $0.35\mu m$ CMOS technology, the linearity error being under a percent for an extended input range and for a small value of the supply voltage $(\pm 3V)$.

Keywords: Active resistor, linearity error, second-order effects

1. INTRODUCTION

CMOS active resistors are very important blocks in VLSI analog designs, mainly used for replacing the large value passive resistors, with the great advantage of a much smaller area occupied on silicon. Their utilisation domains includes amplitude control in low distortion oscillators, voltage controlled amplifiers and active RC filters. These important applications for programmable floating resistors have motivated a significant research effort for linearising their current-voltage characteristic.

The first generation of MOS active resistors (Wang, 1990) used MOS transistors working in the linear region. The main disadvantage is that the realised active resistor is inherently nonlinear and the distortion components were complex functions on MOS technological parameters.

A better design of CMOS active resistors is based on MOS transistors working in saturation (Singh, 1989). Because of the quadratic characteristic of the MOS transistor, some linearisation techniques were developed in order to minimize the nonlinear terms from the current-voltage characteristic of the active resistor. Usually, the resulting linearisation of the $I-V$ characteristic is obtained by a first-order analysis. However, the second-order effects which affect the MOS transistor operation (mobility degradation, bulk effect and channel-length modulation) limits the circuit linearity introducing odd and even-order distortions, as shown in (Sakurai, 1993). For this reason, an improved linearisation technique has to be design in order to compensate also the nonlinearities introduced by the second-order effects.

The original idea for simulating between two pins a linear characteristic current-voltage, similar to the characteristic of a classical resistor, is to pass through these pins the same current, obtained at the output of a differential amplifier and to consider the pins as differential circuit input.

Additionally to its simplicity, the original proposed implementation of the active resistor presents the important advantages of reproducibility and controllability (the value of the entire circuit equivalent resistance could be very easily modified by changing the value of a continuous potential).

The linearity of the classical differential amplifier is relatively poor because of the fundamental nonlinear characteristic of both bipolar and MOS transistors, resulting the possibility of achieving a good linearity only for a restricted input voltage range (the amplitude of the input voltage for the classic differential amplifier using MOS transistors in saturation have to be below a few hundreds of mV). In conclusion, it results the necessity of implementing a linearization technique for decreasing the superior-order nonlinearities of the MOS differential stage and for increasing the available range for the input voltage amplitudes. It exists in literature many circuit techniques used to improve the MOS differential amplifier linearity. It was presented in (Popa, 2000) a third and fifth-order harmonics cancellation with good results and a relatively simple circuit implementation. A constant-sum of the gate-source voltages circuit connection was described in (Hung, 1997) and it allows an important reduction of the total harmonic distortions coefficient of the circuit.
The original proposed differential amplifier is based on a quasi-symmetrical structure, using exclusively MOS devices operating in the saturation region for obtaining a good frequency response. In order to improve the differential structure linearity, an original method of compensating the quadratic characteristic of the MOS transistor working in saturation by two complementary square-root circuits will be implemented.

2. THEORETICAL ANALYSIS

2.1. Original active resistor based on the linear differential structure

The original idea for designing an active resistor is to pass between two pins (V_X and V_Y) a current obtained at the output of a differential amplifier (I_{XY}) and to consider these pins as inputs of the active resistor circuit. This current will be linearly dependent on the differential input voltage, so the equivalent resistance between these two pins will be equal to $1/g_m$ (g_m is the transconductance of the differential amplifier).

$$R_{ECH.} = \frac{V_X - V_Y}{I_{XY}} = \frac{1}{g_m} \tag{1}$$

The block diagram of the original active resistor is presented in Fig. 1.

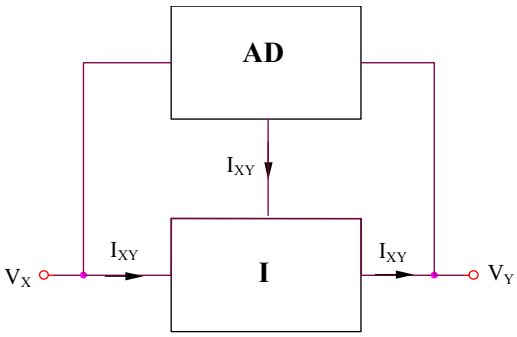

Fig. 1. The block diagram of the active resistor based on a linear differential amplifier

The AD block is a linear differential structure, which will be further analyzed and the I block is a "current pass" circuit. Its goal is to "pass" a current received at its input through two pins (V_X and V_Y). A possible implementation of the current pass block is presented in Fig. 2, consisting in a simple and a multiple current mirrors.

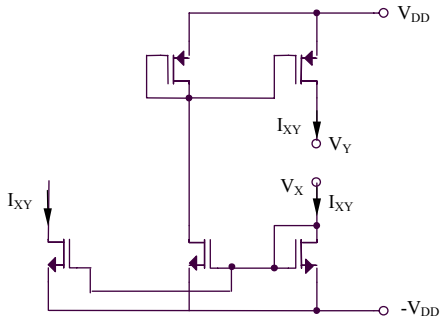

Fig. 2. The current-pass circuit

2.2. Classical CMOS differential amplifier

The most common approach of a differential amplifier in CMOS technology is based on strong-inverted MOS transistors (usually working in the saturation region), having the most important advantage of a much better frequency response comparing to the weak-inverted MOS differential amplifiers. As a result of the quadratic characteristic of a MOS transistor operating in saturation, the transfer characteristic of the classical CMOS differential amplifier will be strongly nonlinear, its linearity being in reasonable limits only for a very limited range of the differential input voltage.
The drain currents of the classical CMOS differential amplifier will have the following nonlinear dependence on the differential input voltage, v_{id}:

$$I_{d_{1,2}} = \frac{I_O}{2} \pm \frac{I_O}{2}\left(\frac{Kv_{id}^2}{I_O} - \frac{K^2 v_{id}^4}{4I_O^2}\right)^{1/2} \tag{2}$$

having a fifth-order limited Taylor expansion around $v_{id} = 0$, expressed by:

$$I_{d_{1,2}}(v_{id}) \cong \frac{I_O}{2} \pm \frac{K^{1/2} I_O^{1/2}}{2} v_{id} \mp$$

$$\mp\frac{K^{3/2}}{16I_O^{1/2}}v_{id}^3\mp\frac{K^{5/2}}{256I_O^{3/2}}v_{id}^5+\ldots \qquad (3)$$

where I_O is the polarization current of the differential amplifier. In order to improve the circuit linearity, especially for large values of the differential input voltage (THD has relatively large values for v_{id} of about hundreds of mV), a linearization technique has to be implemented.

2.3. The original linearized differential amplifier

The proposed differential structure is based on a symmetrical structure that assures, in a first-order analysis, the linearization of the transfer characteristic, equivalent to a constant circuit transconductance.

The original principle for obtaining a linear characteristic of the differential amplifier is to compensate the quadratic law of the MOS transistors biased in saturation region by two complementary square-root circuits, designed using exclusively strong-inverted MOS active devices for improving the circuit frequency response. For the same reason, a current-mode operation of the previous computational circuits will be chosen.

The original square-root circuit is presented in Fig. 3.

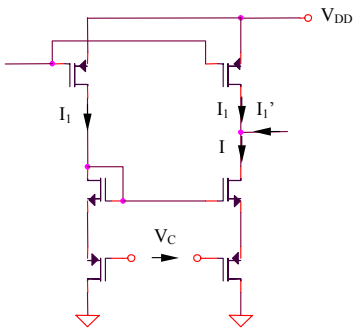

Fig. 3. The original square-root circuit

Considering an operation in saturation of all the MOS transistors from Fig. 3, it is possible to write that:

$$V_C=2\left(V_T+\sqrt{\frac{2I}{K}}\right)-2\left(V_T+\sqrt{\frac{2I_1}{K}}\right) \qquad (4)$$

resulting:

$$\sqrt{I}=\sqrt{I_1}+\sqrt{\frac{K}{8}}V_C \qquad (5)$$

equivalent to:

$$I=I_1+\sqrt{\frac{KI_1}{2}}V_C+\frac{K}{8}V_C^2 \qquad (6)$$

So, the output current of the circuit from Fig. 3 will have the following expression:

$$I_1'=I-I_1=\sqrt{\frac{KI_1}{2}}V_C+\frac{K}{8}V_C^2 \qquad (7)$$

The linear differential amplifier based on the previous described original method is presenting in Fig. 4, consisting in a basic differential structure and two square-root circuits from Fig. 3.

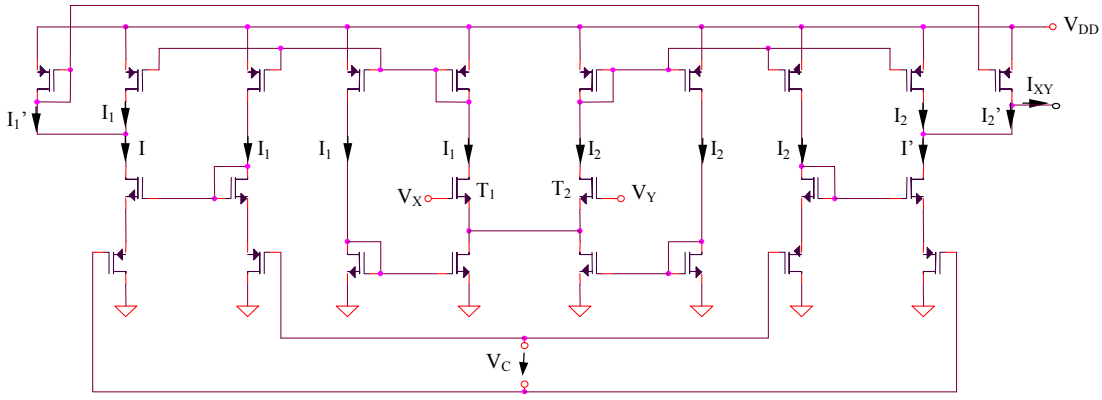

Fig. 4. The linearized differential structure

The output current of the linear differential amplifier presented in Fig. 4 will have the following expression:

$$I_{XY}=I_1'-I_2'=\sqrt{\frac{K}{2}}V_C\left(\sqrt{I_1}-\sqrt{I_2}\right) \qquad (8)$$

Considering a biasing in saturation of T_1 and T_2 transistors, it results:

$$I_{XY}=\frac{KV_C}{2}\left(V_X-V_Y\right) \qquad (9)$$

equivalent to a constant transconductance of the circuit from Fig. 4:

$$g_m=\frac{KV_C}{2} \qquad (10)$$

The important advantages of the previous circuit are the improved linearity that could be achieved in a

first-order analysis and the possibility of controlling the value of the transconductance by modifying a continuous voltage (V_C). The equivalent resistance of the circuit presented in Fig. 1 will have the following expression:

$$R_{ECH.} = \frac{2}{KV_C} \tag{11}$$

covering about two order of magnitude for usual values of K and V_C.

2.4. The second-order effects

The linearity (9) of the transfer characteristic for the differential amplifier from Fig. 4 is slightly affected by the second-order effects that affect the MOS transistor operation, modeled by the following relations: channel-length modulation (12) and mobility degradation (13)).

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{12}$$

$$K = \frac{K_0}{[1 + \theta_G(V_{GS} - V_T)](1 + \theta_D V_{DS})} \tag{13}$$

Considering that the design condition $\lambda = \theta_D$ is fulfilled, the gate-source voltage of a MOS transistor working in saturation at a drain current I_D will be:

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{K}} + \theta_G \frac{I_D}{K} \tag{14}$$

The last term represents the error which affects the quadratic characteristic of the MOS transistor operated in saturation, caused by the previous presented second-order effects. The result will be a small accuracy degradation of the entire circuit linearity, quantitative evaluated by superior-order terms in the transfer characteristic of the differential amplifier:

$$I_{XY} = \sum_{k=1}^{\infty} a_k (V_X - V_Y)^k \tag{15}$$

Because of the circuit symmetry, the even-order terms from the previous relation are usually cancel out, so the main circuit nonlinearity caused by the second-order effects will be represented by the third-order error term from the previous relation, having much smaller value than the linear term.

3. EXPERIMENTAL RESULTS

The low-power CMOS active resistor was implemented in $0.35\mu m$ CMOS technology and the circuit layout is presented in Fig. 5. Because of the original proposed linearization technique, the linearity error of the active resistor could be maintained under a percent for an extended input range.

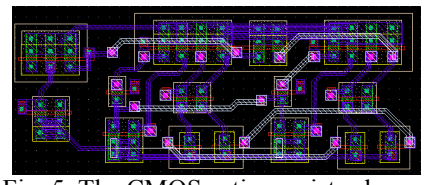

Fig. 5. The CMOS active resistor layout

3. CONCLUSIONS

An original active resistor circuit has been presented. The main advantages of the new proposed implementation are the improved linearity, the small area consumption and the very good frequency response. An original technique for linearizing the $I(V)$ characteristic of the active resistor was proposed, based on the utilization of a new linear differential amplifier and on a current-pass circuit. The linearization of the original differential structure was achieved by implementing an original method for compensating the quadratic characteristic of the MOS transistor working in saturation by two complementary square-root circuits. The errors introduced by the second-order effects has been quantitative evaluated, while the circuit frequency response of the circuit is very good as a result of biasing all MOS transistors in the saturation region and of a current-mode operation of the square-root circuits. The active resistor was implemented in $0.35\mu m$ CMOS technology, the linearity error being under a percent for an extended input range and for a small value of the supply voltage $(\pm 3V)$.

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