A NEW CURRENT-MODE PSEUDO-EXPONENTIAL CIRCUIT WITH AN N-TH ORDER APPROXIMATION

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Abstract: An original implementation in CMOS technology of the exponential function will be presented. In order to improve the circuit frequency response, only MOS transistors working in saturation are used and a current-mode operation is chosen. The compatibility to VLSI designed is achieved by using a FGMOS (Floating-Gate MOS) transistor for reducing the circuit complexity. The approximation error caused by a limited Taylor series expansion is strongly reduced considering a $n-th$ order approximation of the exponential function. Additionally, the $\exp(x)$ function approximation does not depend on technological parameters. The circuit is implemented in $0.35\mu m$ CMOS technology on a die area of about $16\mu m \times 20\mu m$ for the second-order approximation and of $20\mu m \times 35\mu m$ for the $5-th$ order approximation, the resulting approximation error having very small values.

Key words: computational circuit, Taylor series, approximation error, Floating-Gate MOS transistor

1. INTRODUCTION

The exponential circuits are used in telecommunication applications, medical equipment and disk drives (Harjani, 1995; Vlassis, 2000 and 2001; Chang, 2000). In bipolar technology, the exponential function could be easily obtained from the exponential characteristic of the bipolar transistor. These circuits still present important errors because of the nonzero value of the base current, especially for pnp transistors and to the temperature dependence of the bipolar transistor parameters (the thermal voltage is linearly increasing with temperature and the saturation current has an exponential dependence on temperature).
In CMOS technology, the exponential function could be obtained from the characteristic of the MOS transistor working in weak inversion. The great disadvantage of the computational circuits using subthreshold-operated MOS transistors is the poor frequency response caused by the much smaller drain currents available for charging and discharging the parasite capacitances of the MOS transistors. Thus, for circuits realized in CMOS technology that require a good frequency response, only MOS transistors working in strong inversion (usually in saturation) are utilizable. In order to obtain an exponential function using the square characteristic of the MOS transistor in saturation, the new idea is to approximate the exponential function with its $n-th$ order expansion (the polynomial series). The approximation error will be proportional with the amplitude of terms neglected in the expansion.

2. THEORETICAL ANALYSIS

2.1. The exponential circuit with second-order approximation

The new proposed circuit for approximating the exponential function using its expansion in Taylor series (1) is based on classical MOS transistors working in saturation.

$$\exp(x) = 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \ldots \qquad (1)$$

for $x << 1$. Using the ratio of currents I_{IN} and I_O as expansion variable, where I_{IN} is the input current and I_O is the reference current, the expression (1) could be re-written as:

$$I_O \exp\left(\frac{I_{IN}}{I_O}\right) = I_O\left[1+\frac{I_{IN}}{I_O}+\frac{1}{2}\left(\frac{I_{IN}}{I_O}\right)^2+\frac{1}{6}\left(\frac{I_{IN}}{I_O}\right)^3+\ldots\right] \quad (2)$$

The core of the entire circuit, which implements the $n-th$ order approximated exponential function, is the second-order approximated exponential function circuit, presented in this paragraph.

In order to reduce the circuit silicon area by limiting the exponential circuit complexity, a FGMOS (Floating-Gate MOS) transistor will be used, with the result of compatibility with VLSI requirements.

The FGMOS transistor is a MOS transistor whose gate is floating (Fig. 1a), while the symbolical representation of this device is shown in Fig. 1b. The first silicon layer over the channel represents the floating-gate and the second polysilicon layer, located over the floating-gate implements the multiple input gates. This floating-gate is capacitive coupled to the multiple input gates.

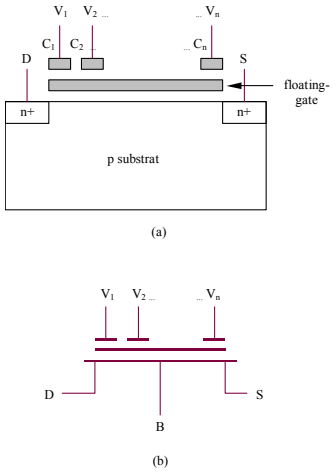

Fig. 1. (a) The basic structure of a n-channel FGMOS transistor; (b) symbolic representation

The drain current of a FGMOS transistor with n-input gates in the saturation region is given by the following relation:

$$I_D = \frac{K}{2}\left[\sum_{i=1}^{n} k_i\left(V_i - V_S\right) - V_T\right]^2 \quad (3)$$

where $K = \mu_n C_{ox}(W/L)$ is the transconductance parameter of the transistor, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, W/L is the transistor aspect ratio, $k_i, i = 1,\ldots,n$ are the capacitive coupling ratios, V_i is the i-th input voltage, V_S is the source voltage and V_T is the threshold voltage of the transistor. The capacitive coupling ratio is defined as:

$$k_i = \frac{C_i}{\sum_{i=1}^{n} C_i + C_{GS}} \quad (4)$$

C_i are the input capacitances between the floating-gate and each of the i-th input and C_{ox} is the gate-source capacitance which is equal to $(2/3)C_{ox}$ for operation in the saturation region. All the overlap capacitances are assumed to be considerably smaller than capacitances summation $\sum_{i=1}^{n} C_i + C_{GS}$.

Equation (3) shows that the FGMOS transistor drain current in saturation is proportional to the square of the weighted sum of the input signals, where the weight of each input signal is determined by the capacitive coupling ratio of the input.

The implementation in CMOS technology of the new proposed pseudo-exponential circuit with second-order approximation is presented in Fig. 2.

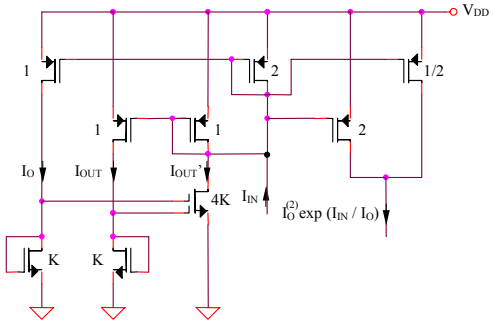

Fig. 2. The pseudo-exponential circuit with second-order approximation

Considering a saturation operation of all MOS transistor from the circuit, the drain current of the FGMOS transistor will have the following expression:

$$I_{OUT}' = \frac{4K}{2}\left[\frac{1}{2}\left(2V_T + \sqrt{\frac{2I_{OUT}}{K}} + \sqrt{\frac{2I_O}{K}}\right) - V_T\right]^2 \quad (5)$$

equivalent to:

$$I_{OUT}' = I_{OUT} + I_O + 2\sqrt{I_{OUT} I_O} \quad (6)$$

Because $I_{OUT}' = I_{OUT} + 2I_O + I_{IN}$, it results that:

$$I_{OUT} = \frac{I_O}{4} + \frac{I_{IN}}{2} + \frac{I_{IN}^2}{4I_O} \quad (7)$$

Using relations (2) and (7), it results a linear expression of the second-order approximated exponential function:

2.2. The original implementation of the exponential circuit with n-th order approximation

For applications that require a better accuracy that could be obtained using the second-order approximation of the exponential function presented above, the circuit proposed in this paragraph uses a $n-th$ order approximation, where n is given by the maximal value of the accepted approximation error. The result will be a tradeoff between the error and complexity.

In order to implement the exponential function with $n-th$ order approximation, n identical circuits from Figure 2 must be used. The input and output currents

for these n circuits and their connection are presented in Figure 3. The "Σ" block implements a linear function for I_{OUT}:

$$I_{OUT} = I_O + I_{IN} + \sum_{k=1}^{n-1} b_k I_{OUT}^{(k)} \quad (9)$$

where b_k are constants coefficients which will be further analyzed.

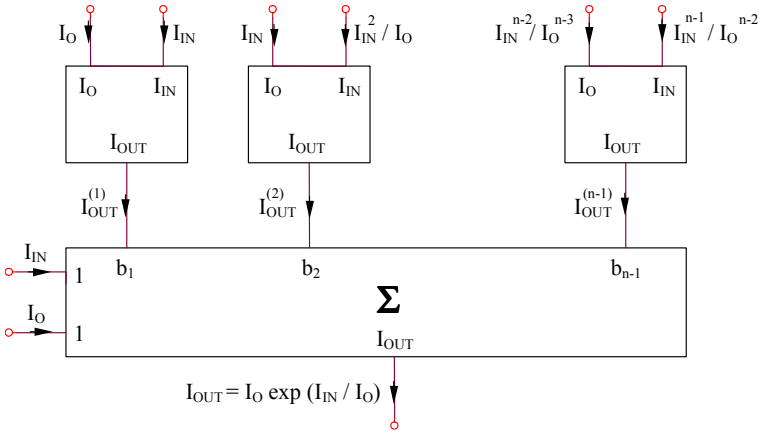

Fig. 3. The block diagram of the $n-th$ order approximated exponential circuit

Using the notation $x = I_{IN} / I_O$, the n output currents of these circuits could be expressed as:

$$I_{OUT}^{(1)} = \frac{I_O}{4}\left(1 + 2x + x^2\right) = \frac{I_O}{4} a_1(x) \quad (10)$$

$$I_{OUT}^{(2)} = \frac{I_O}{4}\left(x + 2x^2 + x^3\right) = \frac{I_O}{4} a_2(x) \quad (11)$$

$$I_{OUT}^{(3)} = \frac{I_O}{4}\left(x^2 + 2x^3 + x^4\right) = \frac{I_O}{4} a_3(x) \quad (12)$$

…

$$I_{OUT}^{(n)} = \frac{I_O}{4}\left(x^{n-1} + 2x^n + x^{n+1}\right) = \frac{I_O}{4} a_n(x) \quad (13)$$

In order to obtain the $n-th$ order approximation of the exponential function using the previous expressions of the output currents, the new idea is to obtain the expression of x^2, x^3, …, x^n as linear function of $a_1(x)$, $a_2(x)$, …, $a_n(x)$, equivalent to linear functions of $I_{OUT}^{(1)}$, $I_{OUT}^{(2)}$,…, $I_{OUT}^{(n)}$.

After some algebraic computations, it results the following expressions of x^2, x^3, …, x^n:

$$x^2 = a_1(x) - (2x + 1) \quad (14)$$

$$x^3 = a_2(x) - 2a_1(x) + (3x + 2) \quad (15)$$

$$x^4 = a_3(x) - 2a_2(x) + 3a_1(x) - (8x + 5) \quad (16)$$

$$x^5 = a_4(x) - 2a_3(x) + 3a_2(x) - 4a_1(x) + (13x + 8) \quad (17)$$

…

$$x^k = a_{k-1}(x) - 2a_{k-2}(x) + 3a_{k-3}(x) + 4a_{k-4}(x) + \ldots$$
$$\ldots + (-1)^{k-1}\left[(5x + 3)(k - 3) + (3x + 2)\right] \quad (18)$$

…

$$x^n = \sum_{k=1}^{n-1} (-1)^{k-1} k\, a_{n-k}(x) +$$
$$+ (-1)^{n-1}\left[(5x + 3)(n - 3) + (3x + 2)\right] \quad (n > 2) \quad (19)$$

In conclusion, the expression of the $n-th$ order approximation of the exponential function could be written as a linear function of $I_O^{(k)}$, $1 \le k \le n$. Because:

$$I_O^{(k)} = \frac{I_O}{4} a_k(x) \quad (20)$$

it results:

$$\exp(x) = 1 + x + \frac{\frac{4}{I_O} I_{OUT}^{(1)} - (2x + 1)}{2!} +$$
$$+ \frac{\frac{4}{I_O}\left(I_{OUT}^{(2)} - 2I_{OUT}^{(1)}\right) + (3x + 2)}{3!} + \ldots \quad (21)$$

Thus, the original $n-th$ order approximation of the exponential function using a limited Taylor series expansion and n identical circuit for second-order approximation of $\exp(x)$ has been developed.

3. EXPERIMENTAL RESULTS

The exponential circuit was implemented in $0.35\mu m$ CMOS technology on a die area of about $16\mu m \times 20\mu m$ for the second-order approximation and of about $20\mu m \times 35\mu m$ for the $5-th$ order approximation of the same function. The layout of the basic exponential circuit (with second-order approximation) and the layout of the $5-th$ order approximation exponential function circuits are presented in Figs. 4 and 5, respectively.

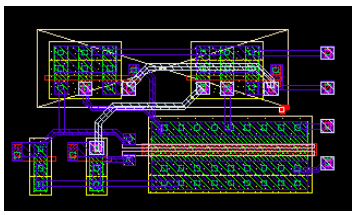

Fig. 4. The layout of the exponential circuit with second-order approximation

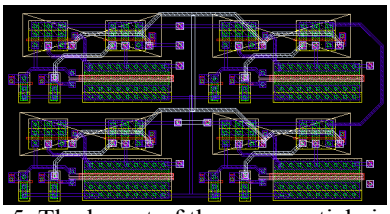

Fig. 5. The layout of the exponential circuit with $5-th$ order approximation

4. CONCLUSIONS

An original implementation in CMOS technology of the exponential function has been presented. In order to improve the circuit frequency response, only MOS transistors working in saturation have been used. The compatibility to VLSI designed is achieved by using a FGMOS transistor for reducing the circuit complexity. The approximation error caused by a limited Taylor series expansion has been strongly reduced considering an $n-th$ order approximation of the exponential function. Additionally, the $\exp(x)$ function is not dependent on technological parameters. The circuit was implemented in $0.35\mu m$ CMOS technology on a die area of about $16\mu m \times 20\mu m$, for the second-order approximation of the exponential function and of about $20\mu m \times 35\mu m$ for the $5-th$ order approximation, the resulting approximation error having very small values.

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