SUPERIOR-ORDER CURVATURE-CORRECTED CMOS VOLTAGE REFERENCE USING A THRESHOLD VOLTAGE EXTRACTOR AND AN ASYMMETRICAL DIFFERENTIAL AMPLIFIER

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Abstract: A new CMOS superior-order curvature-corrected voltage reference will be presented. The first-order correction is achieved by the mutual compensation of the temperature dependencies of threshold voltage and gate-source voltage for MOS transistor working in weak inversion. In order to improve the temperature behavior of the circuit, a new ADA (Asymmetric Differential Amplifier) block will be used for compensating the logarithmic temperature dependence of $V_{GS}(T)$. The voltage reference is implemented in $0.35\mu m$ CMOS technology on a die area of about $20\mu m \times 25\mu m$, the area reduction being achieved by using exclusively MOS transistors. The SPICE simulation confirms the theoretical estimated results, showing a temperature coefficient of $11ppm/K$ for an extended temperature range ($223K < T < 423K$).

Keywords: Temperature dependence, superior-order curvature-correction technique, threshold voltage extractor

1. INTRODUCTION

The reference voltage circuits have a lot of applications in A/D or D/A converters, data acquisition systems, memories or smart sensors.
The earliest high-performance voltage references were implemented in bipolar technology, but, because of the nonlinear temperature dependence of the base-emitter voltage (Filanovsky and Chan, 1996), there exists a theoretical limit for the temperature stability. In order to improve the temperature behavior of the bipolar bandgap reference, a lot of curvature-correction techniques (Popa, 2001; Gunawan, 1993; Lee, 1994) have been developed.
First CMOS bandgap references still used bipolar transistors, realized as parasitic vertical or lateral transistors available in CMOS technology. The result was a small circuit temperature behavior degradation caused by the poorer match of MOS devices' parameters with respect to bipolar transistors.

Latest approaches of CMOS references, using exclusively MOS devices, are based on several classical principles:
- The mutual compensation of the threshold voltage and carriers' mobility temperature dependencies;
- The utilization of the gate-source voltage of a MOS transistor operating in weak inversion as *CTAT* (ComplemenTary with Absolute Temperature) voltage generator;
- The implementation of the *CTAT* voltage using a threshold voltage extractor circuit, which generates the MOS device threshold voltage, with a negative linear temperature dependence.

The new proposed circuit is based on two compensations that assure an important improvement of the circuit thermal behavior:
- The first-order curvature-correction, represented by the mutual compensation of the temperature dependencies of $V_T(T)$ and $V_{GS}(T)$;
- The superior-order (logarithmic) curvature-correction implemented by an ADA block, for compensating the logarithmical dependence on temperature from $V_{GS}(T)$ expression.

2. THEORETICAL ANALYSIS

2.1. The temperature dependence of $V_{GS}(T)$ for a MOS transistor working in weak inversion

Similarly to the bipolar approach, the gate-source voltage represents the simplest implementation in CMOS technology of a *CTAT* voltage, having the great advantage of a very good controllability through the temperature dependence of the operating drain current.
Considering a subthreshold operation of the MOS transistor, its logarithmical law could be expressed as [2]:

$$V_{GS}(T) = V_T(T) + nV_t \ln\left[\frac{I_D(T)}{(W/L)I_{D0}}\right] \quad (1)$$

Most of MOS transistor parameters are depending on temperature: the threshold voltage V_T, the silicon bandgap energy E_G, I_{D0} current (with a temperature dependence given by the continuity between the weak inversion and strong inversion regions) and the thermal voltage V_t. Considering a temperature dependence of the drain current expressed as:

$$I_D(T) = CT^{\alpha} \quad (2)$$

where α is a constant parameter, it results the following expression for the temperature dependence of the gate-source voltage:

$$V_{GS}(T) = V_{FB} + E_G + \frac{V_{GS}(T_0) - V_{FB} - E_G}{T_O}T + \\ + \frac{nkT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_O} \quad (3)$$

T_0 being the reference temperature. The first term is a constant term, the second one is a linear term and the last term models the nonlinearity of the gate-source voltage temperature dependence. This term will be compensated by a suitable logarithmic dependent on temperature term, implemented using an *ADA* block.

2.2. The temperature dependence of $V_T(T)$

The threshold voltage is a very important parameter from MOS transistor model, whose temperature dependence could be expressed as:

$$V_T(T) = m + nT \quad (4)$$

where $m > 0$ and $n < 0$ are constant parameters with respect to temperature variations.
The threshold voltage expression could be obtained using an original threshold voltage extractor circuit, presented in Fig. 1 (all MOS transistor are working in saturation).

The principle of operation is based on the weight difference of gate-source voltages for MOS transistors working in saturation (T_1, T_2, T_3 and T_6). Because T_4 and T_5 transistors are identical and biased at the same drain current, the output voltage expression will be:

$$V_{O_1} = V_A - V_B \quad (5)$$

So, T_4 and T_5 transistors work as a difference circuit. It results:

$$V_{O1} = 3\left(V_T + \sqrt{\frac{I_{D_1}}{K_1}}\right) - \left(V_T + \sqrt{\frac{I_{D_6}}{K_6}}\right) \quad (6)$$

Because $I_{D_1} = I_{D_3}$ and $K_1 = 9K_6$, it results that the circuit from Fig. 1 computes a voltage proportional to the threshold voltage of the MOS devices:

$$V_{O_1} = 2V_T \quad (7)$$

In conclusion, the output voltage V_{O_1} will be linearly decreasing with temperature.

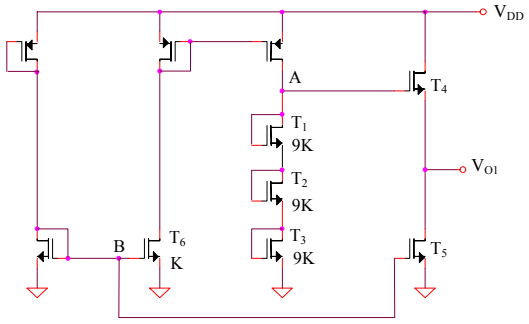

Fig. 1. The CMOS V_T extractor circuit

2.3. The first-order curvature-correction

The original idea for implementing the first-order curvature-correction is to compensate the linear term from $V_{GS}(T)$ expression (3) using the linear decreasing with temperature of the threshold voltage.
The first-order curvature-corrected voltage reference is presented in Fig. 2. T_6 and T_7 transistors act as a difference circuit, so:

$$V_{O_2}(T) = 3V_{GS_8}(T) - 2V_T(T) \quad (8)$$

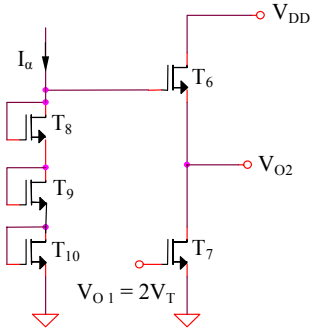

Fig. 2. The first-order corrected voltage reference

$$V_{O_2}(T) = 3(V_{FB} + E_G) + 3\frac{V_{GS}(T_O) - V_{FB} - E_G}{T_O}T +$$

$$+ 3\frac{nkT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_O} - 2(m + nT) \qquad (9)$$

where α is a constant that models the temperature dependence of I_α current:

$$I_\alpha(T) = ct.T^\alpha \qquad (10)$$

The first-order curvature-correction condition is the cancellation of the linear term from (9) expression, which represents the main cause of the temperature dependence of the circuit:

$$3\frac{V_{GS}(T_O) - V_{FB} - E_G}{T_O} = 2n \qquad (11)$$

Considering that the previous design condition is fulfilled, the remaining temperature dependence of the output voltage V_{O_2} will be given only by the logarithmic dependent on temperature term:

$$V_{O_2}(T) = [2(V_{FB} + E_G) - m] + 2(\alpha + \gamma - 2)\frac{nkT}{q}\ln\frac{T}{T_O} \qquad (12)$$

2.4. The superior-order (logarithmic) curvature-correction

The new proposed technique for improving the performance of the voltage reference circuit by removing the logarithmic dependent on temperature term from (12) is to implement a circuit whose difference between output and input voltages is able to compensate this undesired term.

This circuit, named ADA (Asymmetric Differential Amplifier), is presented in Fig. 3.

I_O and I_3 currents are independent on temperature and $PTAT^3$, respectively ($I_3(T) = ct.T^3$). Considering a weak inversion operation of all MOS transistors from the circuit, the difference between output and input voltages could be expressed as:

$$\Delta V_{REF} = V_{REF}^{SUP} - V_{O_2} = -3\frac{nkT}{q}\ln\frac{T}{T_O} \qquad (13)$$

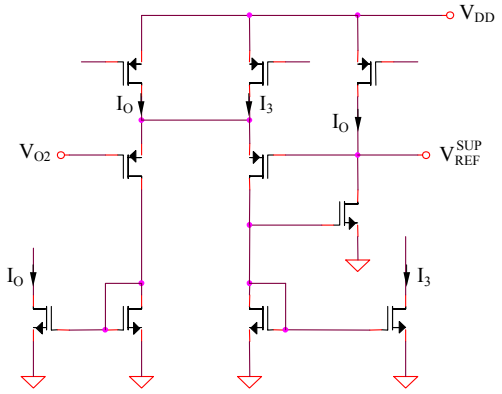

Fig. 3. The Asymmetric Differential Amplifier

Because for the usual value $\gamma = 2$, by biasing T_8, T_9 and T_{10} transistors from Fig. 2 at a $PTAT$ current ($\alpha = 1$), it results (from (12)):

$$V_{O_2}(T) = [3(V_{FB} + E_G) - 2m] + 3\frac{nkT}{q}\ln\frac{T}{T_O} \qquad (14)$$

Thus, the correction term ΔV_{REF} will compensate the logarithmic term from (12), resulting a reference voltage independent on temperature:

$$V_{REF} = 3(V_{FB} + E_G) - 2m \neq V_{REF}(T) \qquad (15)$$

This independence on temperature could be achieved only in a first-order approximation, neglecting the second-order effects that affect the MOS transistor operation (mobility degradation (16), channel length modulation (17) and bulk effect $V_T = V_T(V_{BS})$):

$$K = K_O\frac{1}{1 + \theta_D V_{DS}}\frac{1}{1 + \theta_G(V_{GS} - V_T)} \qquad (16)$$

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad (17)$$

where θ_D, θ_G and λ are constants from the MOS transistor model. Taking into account the second-order effects, the result will be a nonzero value of the temperature coefficient of the reference voltage.

Considering that the design condition $\lambda = \theta_D$ is fulfilled and that θ_G has a relatively small value, the additional errors caused by the second-order effects will have a non-significant effect in the temperature characteristic of the voltage reference circuit. The entire implementation in CMOS technology of the superior-order curvature-corrected voltage reference is presented in Fig. 4.

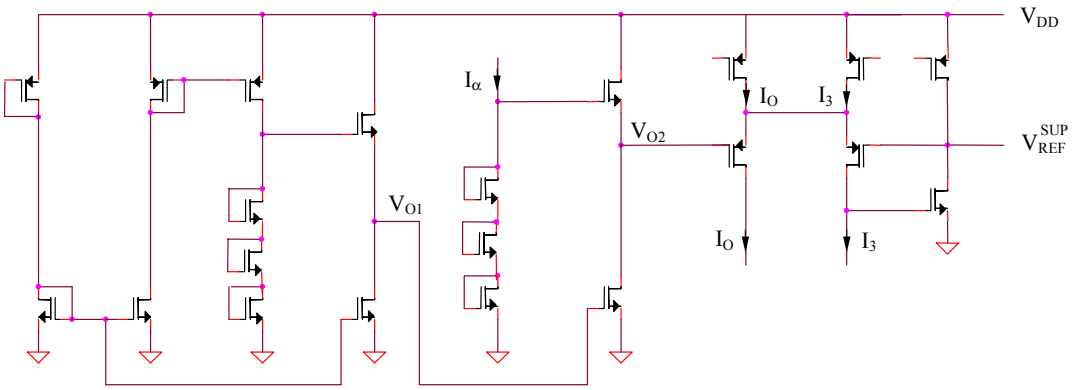

Fig. 4. The superior-order curvature-corrected voltage reference

3. EXPERIMENTAL RESULTS

The SPICE simulation of the temperature dependence of the reference voltage for the circuit presented in Fig. 4 is shown in Fig. 5, showing a temperature coefficient of about $11ppm/K$ for an extended temperature range ($223K < T < 423K$).

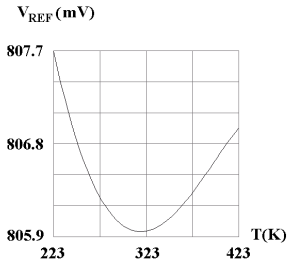

Fig. 5. The SPICE simulation for the superior-order curvature-corrected voltage reference

The layout of the voltage reference, implemented in $0.35\mu m$ CMOS technology on a silicon area of $20\mu m \times 25\mu m$ is presented in Fig. 6.

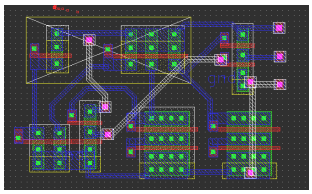

Fig. 6. The layout of the voltage reference

4. CONCLUSIONS

A new CMOS voltage reference with superior-order curvature-correction has been presented. The first-order curvature-correction was achieved by the mutual compensation of the temperature dependencies of threshold voltage and gate-source voltage for a MOS transistor working in weak inversion. In order to improve the temperature behavior of the circuit, a new ADA (Asymmetric Differential Amplifier) block has been used for compensating the logarithmic temperature dependence of $V_{GS}(T)$.

The voltage reference is implemented in $0.35\mu m$ CMOS technology on a die area of about $20\mu m \times 25\mu m$, the area reduction being achieved by using exclusively MOS transistors, that is by removing any resistor from the circuit. The SPICE simulation confirms the theoretical estimated results, showing a temperature coefficient of $11ppm/K$ for an extended temperature range ($223K < T < 423K$), a very good value comparing to other previous reported works.

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