OPTIMUM DESIGN OF FREQUENCY SELECTIVE AMPLIFIER INTENDED FOR CHOPPER STABILIZED APLICATIONS

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Abstract: This paper presents a systematic manual design flow and performance analysis for a frequency selective amplifier (FSA) intended for chopper stabilization applications. The selective amplifier emulates a current driven RLC parallel resonator, implemented using g_mC stages. The FSA was implemented in a standard 0.6 μm process and its performances are checked by SPICE simulation.

Keywords: frequency selective amplifier, chopper stabilization, transconductance stage.

1. INTRODUCTION

This paper analyses a frequency selective amplifier (FSA) optimized for chopper stabilized amplifiers.
Due to the MOS transistors noise and poor matching (Drennan, 2003) precision CMOS amplifiers usually implement offset and noise reduction techniques, as chopper stabilization and autozero (Enz, 1997).

Chopper stabilization requires both signal amplification and filtering, and the FSA use, which combines these two functions, is an efficient solution. One FSA's possible implementation is based on active g_mC filter. This technique is largely used in present day IC design as it offers simple filtering and gain capabilities for a moderate frequency range at reasonable area consumption.

2. CHOPPER STABILISATION TECHNIQUE

This paper focuses on the FSA optimum design. The following chopper stabilization technique short description underlines the special FSA design requirements for chopper applications. (Enz, 1997)

Chopper stabilization uses modulation to separate the signal from the amplifier's offset and low frequency noise. The signal is transferred from its base band to the modulation frequency before the amplifier's noise and offset are summed. A FSA is then used to amplify the signal and reject the offset and low frequency noise. The signal is demodulated and brought back to its base band. The FSA gain should be large enough to reduce the second stage noise and offset contribution.

3. FSA BASIC SCHEMATIC

The FSA presented in this paper (see Fig. 1) is basically a parallel *RLC* resonator driven by a g_mC stage.

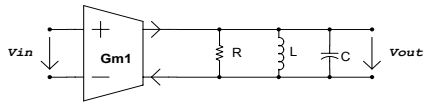

Fig. 1. FSA simplified schematic.

The g_mC stages are also used to implement the resistor and inductor – see Fig. 2.a and b.

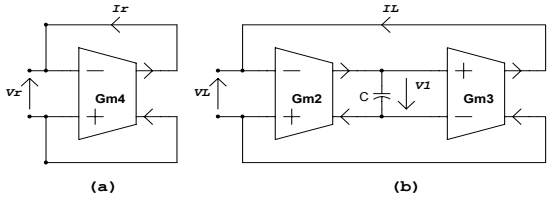

Fig. 2. (a) resistor, and (b) inductor implementation.

$$R_{eq} = 1/g_{mS4}\,,\quad L_{eq} = C/g_{mS2}g_{mS3} \tag{1}$$

By replacing in Fig. 1 the resistor and inductor with their g_mC equivalents results the FSA functional blocks schematic (see Fig. 3)

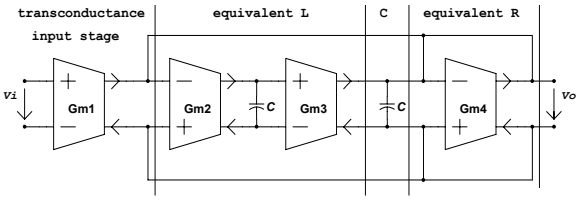

Fig. 3 FSA functional blocks schematic.

4. FSA TRANSFER FUNCTION

From FSA's small signal equivalent circuit (Fig. 4),

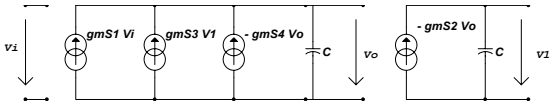

Fig. 4 FSA small signal equivalent circuit

the FSA "ideal" transfer function results[1]:

$$H_i(\mathrm{j}\omega)=\frac{V_o}{V_i}=\frac{\mathrm{j}\omega g_{mS1}/C}{(\mathrm{j}\omega)^2+\mathrm{j}\omega g_{mS4}/C+g_{mS2}g_{mS3}/C^2} \quad (2)$$

We need a narrow bandwidth. To this end, we impose a double pole transfer function. The condition is

$$\Delta=g_{mS4}^2C^2-4g_{mS2}g_{mS3}C^2=0\,,\; g_{mS4}^2=4g_{mS2}g_{mS3} \quad (3)$$

and the double root is given by

$$\omega_0=g_{mS4}/2C \quad (4)$$

The ideal transfer function is:

$$H_i(\mathrm{j}\omega)=\frac{g_{mS1}}{g_{mS4}}\frac{2\,\mathrm{j}\omega/\omega_0}{(1+\mathrm{j}\omega/\omega_0)^2}\,; \quad (5)$$

Fig. 5 shows the "ideal" transfer function Bode plots.

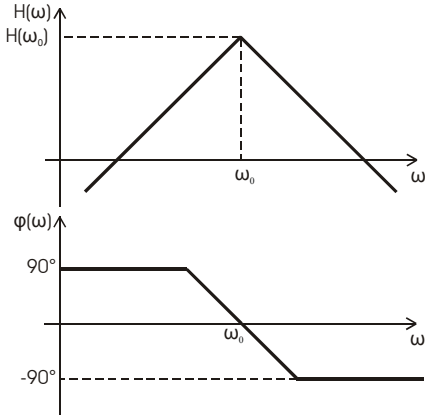

Fig. 5 FSA "ideal" transfer function.

These results support the *RLC* model (see Section 3). The total gain is determined by G_{m1} and R (implemented by G_{m4}). The peak gain magnitude is:

$$H_i(\omega_0)=g_{mS1}/g_{mS4} \quad (6)$$

5. PARASITIC RESISTANCES INFLUENCE

To accurately model the low frequency stage behavior, we must take into account the parasitic resistance effects. The output node is a low impedance node. The only high impedance node is V_1 and we will consider only its parasitic resistance, R_p. The new "real" transfer function results:

$$\frac{H(\mathrm{j}\omega)}{H_i(\omega_0)}=\frac{2\omega_0(\omega_z+\mathrm{j}\omega)}{(\mathrm{j}\omega)^2+\mathrm{j}\omega(\omega_z+2\omega_0)+2\omega_0(\omega_z+2\omega_0)} \quad (7)$$

where

$$\omega_z=1/CR_p\,; \quad (8)$$

[1] G_{mi} is the stage name and $g_{mS\,i}$ is its transconductance.

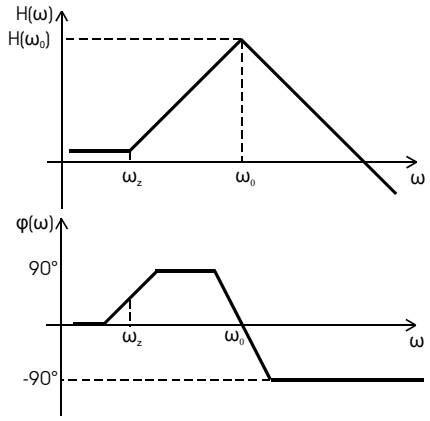

Fig. 6 FSA "real" transfer function

Fig. 6 shows the "real" transfer function Bode plots.

The transfer function's (7) zero is no longer in origin but in ω_z. If $1/R_p$ is small enough, i.e. $\omega_z<<\omega_0$ the natural frequency value is practically unchanged and the transfer function $H(\mathrm{j}\omega)$ can be approximated by

$$\left.\frac{H(\mathrm{j}\omega)}{H_i(\omega_0)}\right|_{\omega_z<<\omega_0}\approx\frac{2\omega_z}{\omega_0}\frac{(1+\mathrm{j}\omega/\omega_z)}{(1+\mathrm{j}\omega/\omega_0)^2} \quad (9)$$

The peak gain magnitude is also unaffected by R_p,

$$H(\omega_0)\big|_{\omega_z<<\omega_0}\approx H_i(\omega_0) \quad (10)$$

6. TRANSCONDUCTANCE STAGES

The peak gain magnitude is given by two stages g_m ratio – equation (6). To get a large g_m ratio, we shall use two different g_m stage topologies: the standard differential pair and a linearized g_m stage.

6.1 Standard Differential Pair

The standard differential pair transconductance stage and its small signal low frequency equivalent circuit are presented in Fig. 7.a, and Fig. 7.b. (Gray, 2001). Applying a $2V_d=V_{inp}-V_{inm}$ differential signal and considering the load resistance, R_L, much smaller than the MN1, MN2 output resistance, r_o, and the bias current sources output resistance, R_b, the output current is $I_o=g_{m1}V_d$. The stage transconductance results

$$g_{mS}=\frac{I_o}{2V_d}=\frac{g_{m1}}{2}=\mu C_{OX}(W/L)_1V_{ov} \quad (11)$$

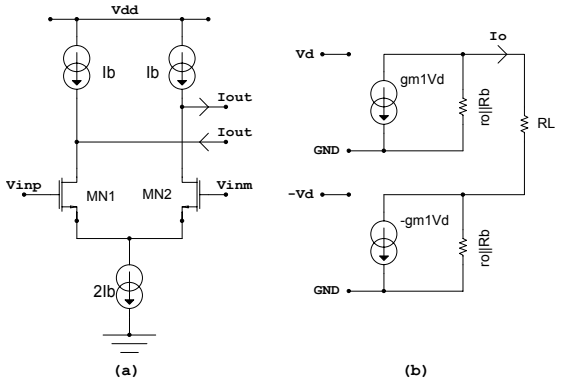

Fig. 7 Standard differential pair.

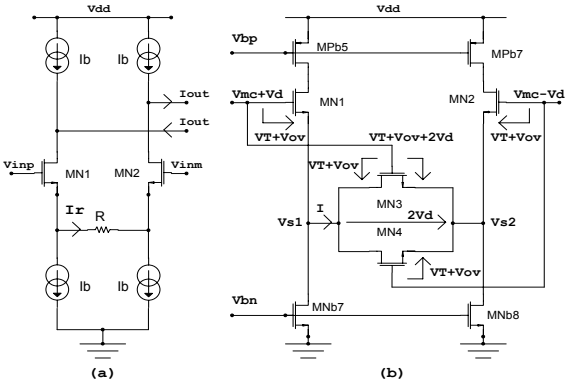

Fig. 8 Linearized g_m stage
(a) principle and (b) implementation

6.2 Linearized Transconductance Stage

Fig. 8.a presents the linearized g_m stage basic schematic. (Krummenacher, 1988) The two differential transistors are identical and biased at the same current I_b, so they work at the same V_{gs}. The differential voltage, $2V_d=V_{inp}-V_{inm}$, appears on R resistor resulting in a $I_r=2V_d/R$ current. This stage is biased from current sources, with a constant I_b current, so I_r must be equal to the output current. The resulting g_m is

$$g_m = I_o / 2V_d = I_r / 2V_d = 1/R \tag{12}$$

We must note that this model is accurate only for small I_d currents. MN1 and MN2 currents are I_b+I_r and I_b-I_r, respectively. So, for large I_r the two differential transistors work at different drain current and the assumption $V_{gs1}=V_{gs2}$ is not verified. A linearized g_m stage implementation that uses MOS transistors instead of resistors (see Fig. 8.b) is described by:

$$V_{gs3} = V_T + V_{ov} + 2V_d \; ; \; V_{gs4} = V_T + V_{ov} \tag{13}$$

$$V_{ds3} = V_{ds3} = 2V_d \tag{14}$$

The MN3 and MN4 transistors are biased in the linear region and their drain currents are

$$I_{D3} = K_3\left[(V_{ov} + 2V_d)2V_d - 2V_d^2\right] \tag{15}$$

$$I_{D4} = K_4\left[2V_{ov}V_d - 2V_d^2\right] \tag{16}$$

where we considered the two transistors identical, with $K_{3,4}=\mu_n C_{OX}(W/L)_{3,4}$. The total current is

$$I_o = I_{D3} + I_{D4} = 4K_3V_{ov}V_d \tag{17}$$

The stage transconductane is in this case

$$g_m = \frac{I_o}{2V_d} = 2\mu C_{OX}(W/L)_3 V_{ov} \tag{18}$$

For the standard differential pair, g_m is controlled by the differential pair transistor geometry [see (11)] while for the liniarized transconductance stage, g_m is controlled by MN3, MN4 geometry.

We note that, for MP3 and MP4, we cannot discern between source and drain. If the input signal polarity changes, the source and drain change places. This is why we cannot connect MP3 and MP4 bulk to the source so we connect it to the highest potential, V_{dda}.

This leads to a threshold voltage increase base on the "bulk effect" (Razavi, 2001; Gray, 2001). In determining the stage transconductance, we assumed all *p* channel transistors have the same threshold voltage (see Fig. 8.b). If MP3 and MP4 have higher V_T they will not work at the same overdrive as the differential pair and equation (18) will no longer be accurate. It is even possible that MP3 and MP4 remain in the "off" region if the V_T is high.

This is why we shall also connect the MP1 and MP2 bulk to V_{dda}. This way, MP1, Mp2, MP3 and MP4 have the same bulk–source voltage and, consequently, the same V_T.

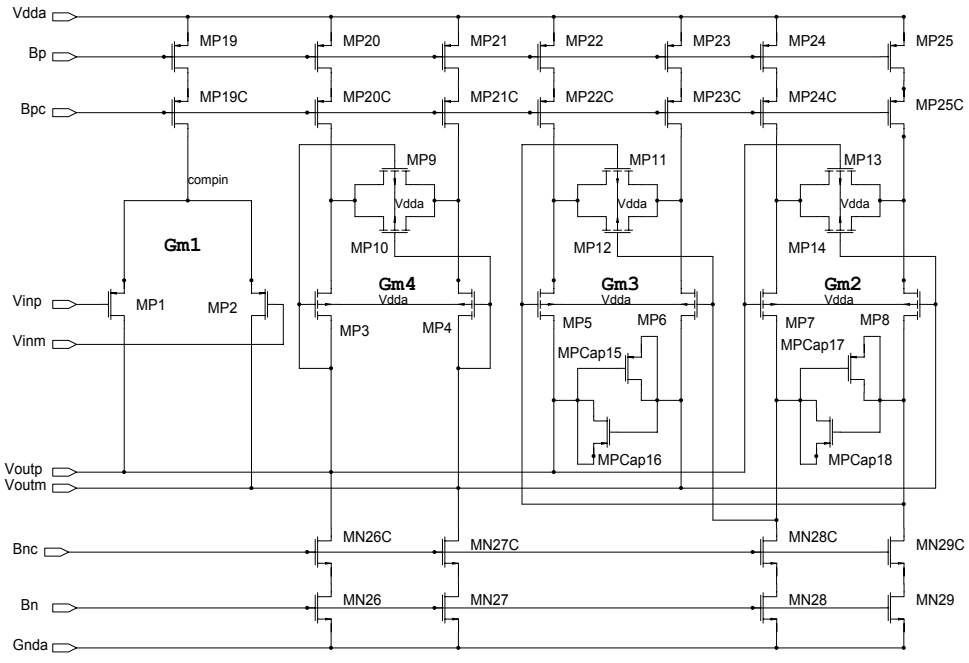

Fig. 9 FSA complete schematic

7. FSA DESIGN

Fig. 9 presents the FSA schematic. (Enz, 1997) The input stage, G_{m1}, uses a standard differential pair, but the other stages use the linearized topology, to get a high g_{mS1}/g_{mS4} ratio. We use cascode current mirrors as they provide high output impedance.

We underline the difference between $g_{mS1\text{-}4}$ that are the $G_{m1\text{-}4}$ stages transconductances and $g_{m1\text{-}4}$ that are the MP1–MP4 transistors transconductances.

Also, we underline that MP9–MP14 transistors have the bulk connected to V_{dda} as their source and drain are not predetermined. MP3–MP8 also have their bulk connected to V_{dda} in order to have the same "bulk effect" and thus the same threshold voltage as MP9–MP14 (see Section 6.2)

7.1 FSA peak gain

The FSA peak gain is given by (6) see Section 4. The G_{m1} stage is a standard differential pair with

$$g_{mS1} = \frac{g_{m1}}{2} = \frac{1}{2}\sqrt{2\mu_p C_{OX}(W/L)_1 I_{D1}} \tag{19}$$

G_{m4} is a liniarized g_m stage, with g_{mS4} given by (18). We express V_{ov4} as a function of I_{D4}, and get

$$g_{mS4} = \sqrt{2\mu_p C_{OX}\frac{(W/L)_9^2}{(W/L)_4} I_{D4}} \tag{20}$$

The FSA peak gain results

$$H(\omega_0) = \frac{g_{mS1}}{g_{mS4}} = \sqrt{\frac{(W/L)_1(W/L)_4}{(W/L)_9^2}}\sqrt{\frac{I_{D1}}{I_{D4}}} \tag{21}$$

We choose the same (W/L) ratio for all differential pairs (simple and linearized), so we have

$$(W/L)_1=(W/L)_4 \tag{22}$$

The peak gain results

$$H(\omega_0) = \frac{(W/L)_1}{(W/L)_9}\sqrt{\frac{I_{D1}}{I_{D4}}} \tag{23}$$

We choose the bias currents I_{D1}=9 µA and I_{D4}=1 µA. For all differential pairs we use L=10 µm, W=20 µm and m=4. For MP9 and MP10, we choose L_9=20 µm and W_9=1 µm. We get $H(\omega_0) = 240$.

To have a double pole at ω_0 frequency, we must fulfill equation (3). We choose

$$g_{mS2} = g_{mS3} = g_{mS4}/2 \tag{24}$$

This leads to L_{11}= L_{13}=10 µm, W_{11}= W_{13}=1 µm.

7.2 FSA offset estimation

As a first order approximation, we consider that the FSA input offset voltage is only given by the differential pair transistors threshold voltages, V_T, mismatch. The threshold voltage variation is described by the Gaussian distribution with the dispersion:

$$\sigma(\Delta V_T) = \frac{AVT0}{\sqrt{WL}} \tag{25}$$

where AVT0 is a process parameter. We consider

$$V_{OS} = \Delta V_{T\,max} = 3\sigma(\Delta V_T) \tag{26}$$

With the chosen the transistor size, V_{OS} value results of about 2 mV.

7.3 FSA resonance frequency

The FSA double pole frequency, $\omega_0=g_{mS4}/2_C$, was determined in Section 4. We are interested in the capacitance needed to get the desired frequency:

$$C = \frac{g_{mS4}}{\omega_0} = \frac{g_{mS4}}{2\pi f_0} \tag{27}$$

The G_{m4} stage transconductance is given by (20) and, using the transistor geometry determined in Section 7.1, and $\mu_p C_{OX}$=30 µA/V, we get

$$g_{mS4} = \sqrt{2\times 30\times\frac{0.1^2}{8}\times 1} = 0.272\ \mu\text{A/V} \tag{28}$$

We choose f_0=10 kHz (ω_0=62.8 kHz). This leads to

$$C = \frac{0.272\times 10^{-6}}{62.8\times 10^3} = 4.33\ \text{pF} \tag{29}$$

Using C_{OX}=2 fF/µm^2, the estimated capacitor area is

$$WL = \frac{C}{C_{OX}} = \frac{4.33\ \text{pF}}{2\ \text{fF}/\mu\text{m}^2} = 2165\ \mu\text{m}^2 \tag{30}$$

This capacitor model does not take into consideration important effects, as the overlap capacitance. Also, we did not take into account the differential pairs capacitance that is also important because of the differential pair large area. This is why this area is fit only as a first estimation and must be adjusted by SPICE analysis.

7.4 Current Mirror Design

The current mirror transistors, MP19–MP24 and MN26–MN29 provide the FSA bias current. From matching reasons, each of this transistors should be implemented using the same elementary transistor and with a multiplicity according to the desired current. In this paper we used a L_p=3 µm, W_p=10 µm and L_n=3 µm, W_n=5 µm for all p respectively n channel current mirror transistors.

The current mirror cascode transistors, MP19C–MP24C and MN26C–MN29C are implemented in the same manner.

The differential pairs should be biased symmetrically, so we have

$$\begin{aligned} &m_{20} = m_{21},\ m_{22} = m_{23},\ m_{24} = m_{25} \\ &m_{26} = m_{27},\ m_{28} = m_{29} \end{aligned} \tag{31}$$

MN6 and MN7 take all the G_{m1}, G_{m3}, G_{m4} stages bias current, provided by MP19–MP23 (see Fig. 9). MN28 and MN29 take the bias current from G_{m4} stage, provided by MP24 and MP25. This leads to the following multiplicity relationships

$$\begin{aligned} &m_{26} = (m_{19}/2) + m_{20} + m_{22} \\ &m_{28} = m_{24} \end{aligned} \tag{32}$$

8. FSA SPICE ANALYSIS

8.1 Transfer Function

The SPICE simulated (Tsividis, 1999) FSA transfer function is presented in Fig. 10. The resulted peak gain magnitude of 256 compares well to the manually estimated value of 240.

We used the estimated capacitor area [see equation (30)] as a first iteration and the resulted resonance frequency was 6.9 kHz. We adjusted the capacitor area to 1296 μm^2, to get the desired resonance frequency of about 10 kHz.

The finite zero frequency (ω_z=4.59 Hz) introduced by the parasitic resistor is clearly visible in Fig. 10. We note that the $\omega_z << \omega_0$ condition is fulfilled.

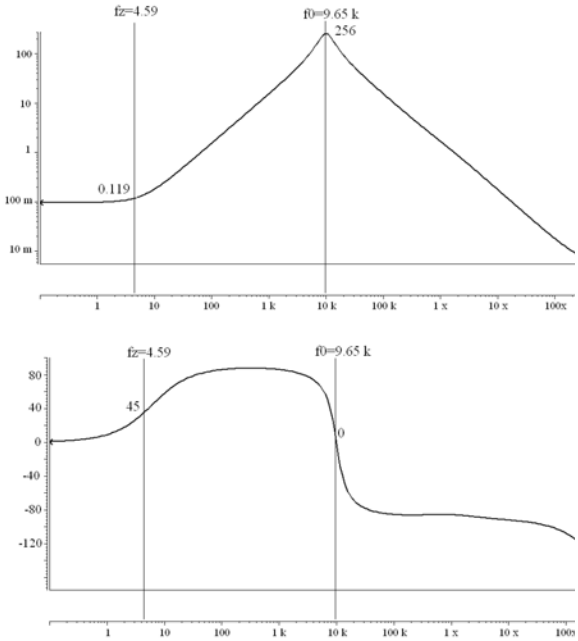

Fig. 10 SPICE simulated a) module and b) phase FSA transfer function

We can use ω_z to estimate the parasitic resistances introduces by the current mirrors. From (8) we have

$$R_p = \frac{1}{C\omega_z} = \frac{1}{4.33\times10^{-12}\times 4.59} \cong 8\ \text{G}\Omega \qquad (33)$$

8.2 FSA Gain Analysis

The FSA gain (see Section 7.1) is given by

$$H(\omega_0) = \frac{(W/L)_1}{(W/L)_9}\sqrt{\frac{I_{D1}}{I_{D4}}} \qquad (34)$$

As we can see, H(ω_0) is determined by four parameters: $(W/L)_1$, $(W/L)_9$, I_{D1} and I_{D4}. In this section we analyze the accuracy of this manual model in rapport to each parameter variation.

First we consider the H(ω_0) versus $(W/L)_1$ dependency. The manual estimated and SPICE simulated H(ω_0) values are presented in Fig. 11 showing a good agreement (relative error less than 15%) for $(W/L)_1$ values up to 15. All other parameters were kept constant: $(W/L)_9$=0.1, I_{D1}=9 μA and I_{D4}=1 μA.

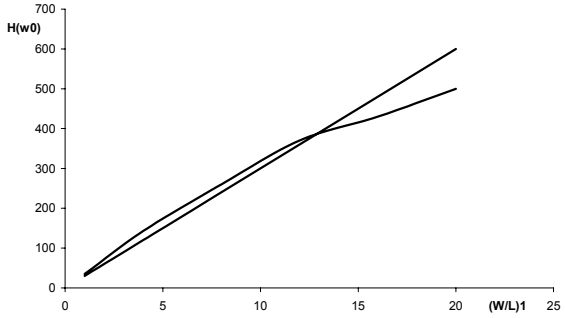

Fig. 11 $H(\omega_0)$– $(W/L)_1$ dependence

For larger $(W/L)_1$ values the differential pair overdrive is very small and the strong inversion model used in our manual analysis is no longer accurate.

We shall now analyze the $H(\omega_0)$ versus $(W/L)_9$, dependency (see Fig. 12). We kept W_9=1 μm and change the L_9 value in the 2…20 μm range. This resulted in a 0.5 to 0.05 $(W/L)_9$ ratio variation. The other parameters were constant: $(W/L)_1$=8, I_{D1}=9 μA and I_{D4}=1 μA.

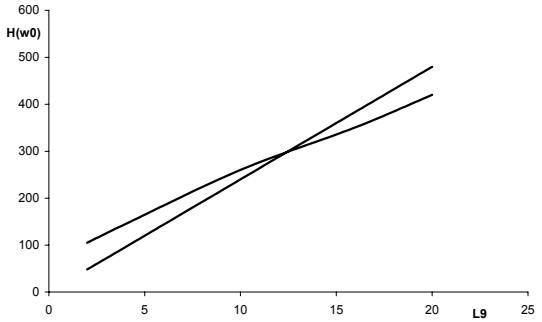

Fig. 12 $H(\omega_0)$–$(W/L)_9$ dependence.

The manual analysis offered good results for the entire analyzed domain.

The $H(\omega_0)$ versus I_{D1} is presented in Fig. 13 where we used the following transistors' size and current: $(W/L)_1$=8, $(W/L)_9$=0.1 and I_{D4}=1 μA.

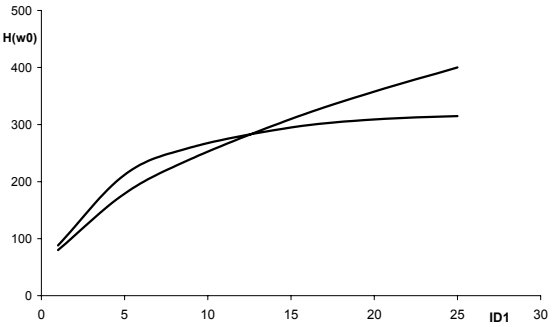

Fig. 13 $H(\omega_0)$– I_{D1} dependence

The model is accurate at low currents. For larger currents values (in this case I_{D1} larger than 20 μA) SPICE simulation predicts a $H(\omega_0)$ saturation effect not predicted by the manual model.

The $H(\omega_0)$ versus I_{D4} is presented in Fig. 14 where we used the following transistors' size and current: $(W/L)_1$=8, $(W/L)_9$=0.1 and I_{D1}=9 μA.

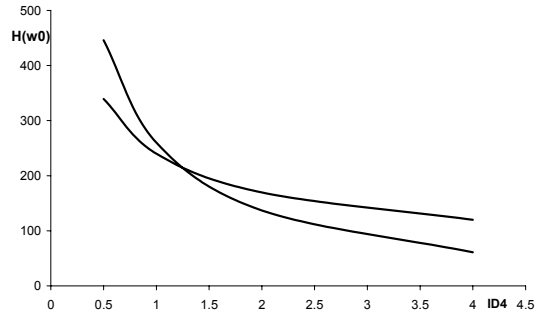

Fig. 14 $H(\omega_0)$–I_{D4} dependence

An important observation is that the FSA peak gain magnitude, $H(\omega_0)$, only depends on transistor geometry ratio and on bias currents ratio – it is independent of process parameters like μC_{OX} or transistors output resistance.

This fact explains the $H(\omega_0)$ manual evaluation accuracy. Indeed, SPICE simulation results differs no more than ±20% from manual estimation results for a wide parameter range.

8.3 FSA Noise Analysis

Noise simulation results (both input and output referred noise) are presented in Fig. 15. (Liu, 2001; Tsividis, 1999)

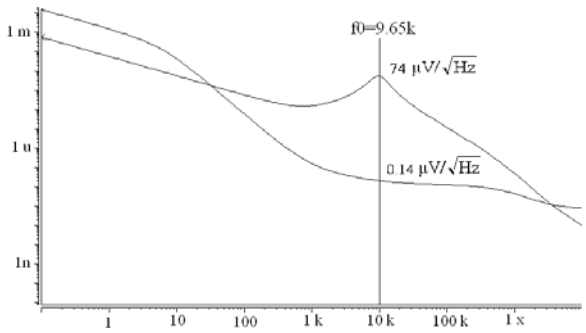

Fig. 15 Input and output equivalent noise

The input referred noise is obtained by dividing the output noise to $H(\omega)$ (see Fig. 10.a). This explains why the input referred noise is larger than the output noise at low frequency, (where $H(\omega)<1$) and becomes smaller at 64 Hz, where $H(\omega)=1$.

The output equivalent noise has a local maximum at the resonance frequency. This is normal because, at this frequency, the input transistor noise is transferred to the output multiplied by the peak gain, $H(\omega_0)$. We are mainly interested in the input equivalent noise value around the resonation frequency, as this noise is directly superposed over the signal. In our application, the input equivalent noise voltage at the resonance frequency is $0.14\ \mu V/\sqrt{Hz}$.

It is important to remember that the relatively high noise value from low frequency, compared to the resonance frequency noise value, has little importance in chopper stabilization technique, as the output signal is demodulated (so the noise low frequency noise is brought to a high band) and than filtered.

9. CONCLUSIONS

In this paper, we present the main design issues and an extended performance analysis for a frequency selective amplifier (FSA) intended for chopper stabilization applications.

The FSA designed in this paper is based on an equivalent *RLC* parallel resonator, implemented using g_mC stages. We provide a simple manual model for the FSA frequency behavior – the FSA transfer function has a double pole at a design controlled frequency and a low frequency zero, that depends on the parasitic resistances. The peak gain value is determined by two transconductance stages g_m ratio.

In this paper, we used two different transconductance stage topologies: the simple differential pair and the liniarized transconductance stage; in order to get a high g_m ratio. Models suitable for manual analysis were presented for both topologies.

We highlighted the main concerns in FSA design: peak gain magnitude estimation, offset estimation, resonance frequency control and current mirrors design.

The manual estimation model results were backed up by SPICE simulation. We analyzed the peak gain variation – manual model versus spice simulation – and the results were in good agreement over a wide design parameters range.

The amplifier designed in this paper has a resonation frequency of about 10 kHz with 256 peak gain. The estimated input equivalent offset voltage is 2 mV.

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