PARASITICS ACCOMMODATION IN THE CLASS-E POWER AMPLIFIER DESIGN

Alexandru NEGUȚ[1], Roland PFEIFFER[2], Alexandru NICOLIN[3], Mircea BODEA[1], Claudius DAN[1]
E-Mail: alex.negut@gmail.com

[1] *"POLITEHNICA" University of Bucharest, Faculty for Electronics, Telecomm. and IT*
[2] *University of the Federal Armed Forces, Munich, Institute for Electronics*
[3] *University of Copenhagen, Faculty of Science*

Abstract: This paper presents a class-E power amplifier (PA) new design algorithm optimized for monolithic implementation. This algorithm accommodates simultaneously the parasitic ground inductance, the switch on-resistance, and the shunt capacitor finite Q-factor value offering an exact solution. For total power dissipation calculation, the effects of the finite turn-off time are also considered. A class-E PA (targeted specifications correspond to a UMTS transceiver, f=1.95 GHz, P_{out}=0.5 W) was designed following the algorithm proposed in this paper. The simulation results fit well the theoretical solution.

Keywords: Communication Systems, RF Power Amplifier, Class-E

1. INTRODUCTION

The class-E PA is a switching-mode amplifier which could provide, under ideal conditions, 100% efficiency. At low frequencies, a MOS transistor could easily model the ideal switch. Above this frequency range the effects of both transistor's switching time (which becomes a significant percentage of the RF cycle) and the device parasitics become important, therefore decreasing the amplifier's efficiency. However, the current and the voltage waveforms of a class-E PA are such that even a transistor with relatively slow switching characteristics leads to good performance (Cripps, 1999). Moreover, when carefully designed and constructed, the class-E PA has greater efficiency than a conventional one (class A, B or C), thus recommending it for mobile applications.

Today's efforts are being focused on the total integration of a wireless transceiver, targeting the "System-on-Chip" level. Since CMOS technology is widely spread and offers the advantage of rather easy implementation of the mixed-signal circuits, the natural next step is the attempt to realize the RF front end, including the power amplifier, on the same die. Present day typical implementations use different chips, manufactured based on different processes, together with discrete elements, thus leading both to price increase and reliability decrease. Therefore, a totally integrated CMOS system-on-chip operating at high frequencies would bring remarkable advantages (Hella and Ismail, 2002).

The issue of the parasitics arises both in a monolithic and a discrete implementation. Typical approaches try to minimize the parasitics values, in order to diminish the losses. In (Milosevic; Kazimierczuk and Puczko, 1987; Zulinski and Steadman, 1987) it is shown that the class-E network can be designed in order to accommodate different non-idealities. Unfortunately, an analytical method for incorporating all their effects cannot be developed, since the resulting equations are non-linear and very complex. In this paper, we focus on developing an algorithm for calculating a class-E network which takes into account the simultaneous presence of a ground inductance and switch and shunt capacitor losses.

The paper is structured as follows: Chapter 2 reviews the class-E design under ideal conditions. A new method developed for the evaluation of the monolithic implemented network's elements when losses

are present is explained in Chapter 3. In Chapter 4 the simulation results are synthesized and in Chapter 5 the conclusions are summarized.

2. THE CLASS-E PA OPERATION UNDER IDEAL CONDITIONS

The class-E PA basic circuit (fig. 1 without r_{on}, L_{sw}, r_C) consists of an active device (operating as a switch), a capacitor C that shunts the switch, a L_0C_0 resonator in series with the load resistance R_L and an excess reactance L. The circuit is supplied through a RF choke L_{RF}.

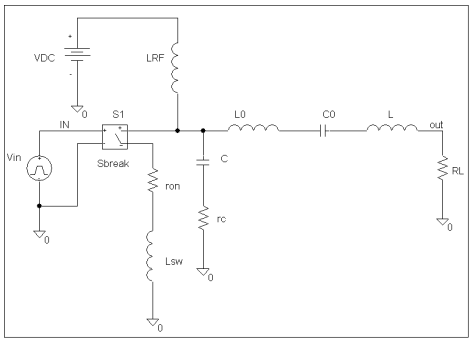

Fig. 1: Class E PA with non-ideal elements (discrete implementation).

For the ideal-case operation analysis the following assumptions have to be made:

- The active device operates as an ideal switch (during the on-state its resistance is zero and can support the entire current flowing through it, while in the off-state its resistance is infinite and can support the voltage that drops on it);
- The switch closes and opens instantaneously;
- The switch is operated at 50% duty-cycle by a squarewave input signal;
- The RF choke inductance is sufficiently large, to allow only the DC current to flow through it;
- The Q-factor of the series LC resonator is large enough, so that only a sinusoidal current can flow through the load.

The way the analysis is being performed is well covered by the literature (Cripps, 1999; Milosevic) and the design equations can be summarized as follows:

$$R_L = 0.577\frac{V_{DC}^2}{P_{out}} \qquad C = 0.318\frac{P_{out}}{\omega V_{DC}^2}$$

$$L = 0.665\frac{V_{DC}^2}{\omega P_{out}} \qquad L_0 = \frac{Q_L R_L}{\omega}$$

$$C_0 = \frac{1}{\omega Q_L R_L} \qquad I_{RF} = 1.862\frac{P_{out}}{V_{DC}}$$

$$I_{DC} = \frac{P_{out}}{V_{DC}} \qquad V_{pk} = 3.563 V_{DC}$$

where I_{RF} is the amplitude of the current in the RLC branch, I_{DC} is the current absorbed from the DC power supply and V_{pk} is the peak voltage on the switch. The current and voltage waveforms, for example for the case f=1.95 GHz, V_{DC}=2.2 V, P_{out}=0.5 W, can be seen in figure 2. These waveforms show the so called "soft-switching" feature of the class-E amplifier: the switch closes when the voltage across it is zero, which means that the shunt capacitor is already discharged and the current through the capacitor crosses zero. In this way, there is no overlap of current and voltage drop on the switch which could result in power dissipation. However, the switch opens when a significant amount of current flows through it and this current must be instantaneously overtaken by the shunt capacitor. In reality, due to the non-idealities of the switch (such as the finite current fall-time), this process is associated with power loss, as shown later.

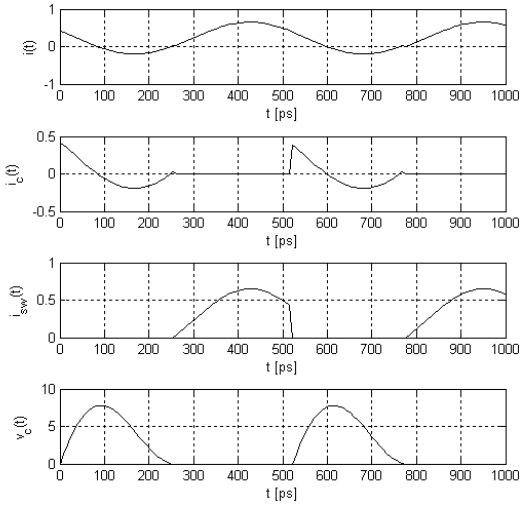

Fig. 2: Current and voltage waveforms for the design example.

It is important to note that the class-E PA offers the advantage of 100% theoretical efficiency, but comes with two major drawbacks. First, being a switching-type amplifier, it is highly nonlinear. Fortunately, with a proper linearization technique, also amplitude modulated signals can be successfully amplified. The second major disadvantage is the peak voltage on the switch. For a class-E PA, high breakdown voltage processes are required. For a discrete implementation this should be not a difficulty, but the high-speed CMOS devices have low breakdown voltage. In this case, the only solution is to lower the supply voltage, but this will result in further decrease of the load resistance value, thus making the impedance transformation to 50 Ω more difficult.

3. DESIGN OF THE CLASS-E PA WHEN LOSSES ARE PRESENT

The operation of the class-E PA under real conditions is affected by parasitics (figure 1) which alter the ideal current and voltage waveforms and lead to losses (i.e., efficiency reduction). In (Milosevic), an

analysis of different losses in the class-E PA is performed for each case separately. Also, in (Raab and Sokal, 1978; Milosevic) the losses associated with ground inductance were estimated in a way more appropriate for discrete implementation. *In this section we shall show that an improved method for the design of the class-E network is possible, dealing with more parasitics simultaneously and accommodating the ground inductance.* The chosen topology (figure 3) is appropriate for integrated circuits, since both the transistor and shunt capacitor share the same ground connection.

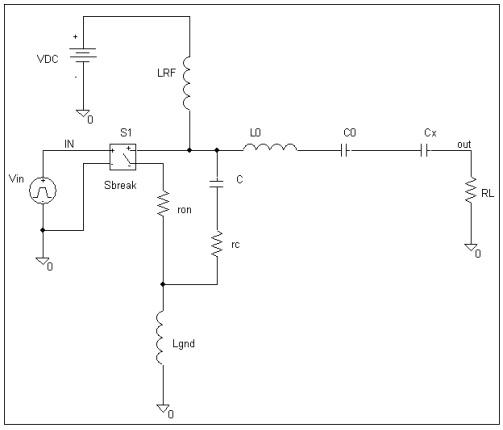

Fig. 3: Class-E PA with non-ideal elements (monolithic implementation).

3.1 Analysing the class-E PA when losses are present

In a discrete implementation (as shown in figure 1), when used as a switch, the MOS transistor will display during the on-state a non-zero on-resistance r_{on} and a parasitic series inductance L_{sw} (due to the parasitics of the transistor package and lead wires). The power loss in this inductor will occur when the switch opens (Raab and Sokal, 1978). At this instant, a significant current flows through the switch (and through L_{sw} as well) and the energy stored in the inductor is being lost. This process repeats itself every RF cycle.

The turn-off time of the transistor must also be taken into account and the effect of a non-zero parasitic series resistance r_C of the shunt capacitor will be added (thus modeling the finite value of the quality factor of the capacitor). Of course, also the ground connection of the shunt capacitor C will display a parasitic inductance, but this can be tuned out by choosing an appropriate value for the capacitance.

When dealing with a monolithic implementation, the difference occurs for the parasitic ground inductance: both the transistor and the shunt capacitor will share the same connection (figure 3). More, the output capacitance of the transistor can be big enough in order to provide the entire needed shunt capacitance. In this case, the switch and the shunt capacitor cannot be any more physically separated.

The analysis performed in this paper will consider only the monolithic case and will include all the effects of r_{on}, r_C and L_{gnd} at once. Because of the non-zero value of r_C, an additional voltage will drop on the shunt capacitor during the off-state of the switch. On the other hand, the presence of r_{on} leads to voltage drop on the switch during its on-state. On L_{gnd} a sinusoidal voltage will drop, since the currents combining in this branch form a sinusoidal waveform with an offset.

The currents through the switch and the shunt capacitor will be considered as the ones in the ideal case, although this approach is not very rigorous. The errors thus made can be neglected:

$$i_{sw}(t) = \begin{cases} 0; \omega t \in [0,\pi) \\ I_{DC} + I_{RF}\sin(\omega t + \varphi); \omega t \in [\pi, 2\pi) \end{cases}$$

$$i_C(t) = \begin{cases} I_{DC} + I_{RF}\sin(\omega t + \varphi); \omega t \in [0,\pi) \\ 0; \omega t \in [\pi, 2\pi) \end{cases}$$

Since the current flowing through the parasitic ground inductance is:

$$i_{gnd}(t) = i_{sw}(t) + i_C(t)$$

the voltage drop on L_{gnd} can be expressed as:

$$v_{Lgnd}(\theta) = L_{gnd}\omega\frac{\mathrm{d}i(\theta)}{\mathrm{d}\theta} = L_{gnd}\omega I_{RF}\cos(\theta + \varphi)$$

where $\theta = \omega t$. Since the switch shunts the capacitor, its voltage waveforms will not be affected by the presence of the ground inductance.

During the on-state of the switch, due to r_{on}, the voltage drop on the shunt capacitor is no longer zero:

$$v_C(\theta) = i_{sw}(\theta) r_{on}$$

When the switch opens at the moment θ_{open}, the initial voltage of the capacitor will be:

$$V_{iC} = i_{sw}(\theta_{open}) r_{on} = \left[I_{DC} + I_{RF}\sin(\theta_{open} + \varphi)\right] r_{on}$$

During the off-state of the switch, the voltage drop on the shunt capacitor is:

$$v_C(\theta) = \frac{1}{\omega C}\int_0^{\theta} i_C(\theta)\mathrm{d}\theta + r_C i_C(\theta) + V_{iC} \qquad (1)$$

For simplicity, we consider the moment of switch opening is $\theta_{open}=0$ and solving (1) leads to:

$$v_C(\theta) = \frac{1}{C\omega}\left[I_{DC}\theta - I_{RF}\cos(\theta + \varphi) + I_{RF}\cos\varphi\right] +$$
$$+ r_C\left[I_{DC} + I_{RF}\sin(\theta + \varphi)\right] + \left(I_{DC} + I_{RF}\sin\varphi\right) r_{on}$$

The voltage across the switch is:

$$v_C(\theta) = \begin{cases} \frac{1}{C\omega}\left[I_{DC}\theta - I_{RF}\cos(\theta + \varphi) + I_{RF}\cos\varphi\right] + \\ + r_C\left[I_{DC} + I_{RF}\sin(\theta + \varphi)\right] + \\ + \left(I_{DC} + I_{RF}\sin\varphi\right) r_{on}; \theta \in [0,\pi) \\ \left[I_{DC} + I_{RF}\sin(\theta + \varphi)\right] r_{on}; \theta \in [\pi, 2\pi) \end{cases} \qquad (2)$$

Now we shall apply the class-E conditions to the switch-capacitor loop:

$$v_C(\pi) = 0$$

$$\left.\frac{\mathrm{d}v_C(\theta)}{\mathrm{d}\theta}\right|_{\theta=\pi} = 0$$

and we get:

$$\begin{cases} \dfrac{I_{DC}\pi + 2I_{RF}\cos\varphi}{C\omega} + I_{DC}(r_{on}+r_C) + I_{RF}(r_{on}-r_C)\sin\varphi = 0 \\ \dfrac{I_{DC} - I_{RF}\sin\varphi}{C\omega} - I_{RF}r_C\cos\varphi = 0 \end{cases}$$

resulting the solution for φ:

$$\tan\varphi = -\frac{\pi r_C C\omega + 2 + (C\omega)^2 r_C(r_{on}+r_C)}{\pi + 2r_{on}C\omega} \qquad (3)$$

The transistor drain voltage will be now the sum between the drain-to-source voltage (2) and the voltage drop on the ground inductance:

$$v_t(\theta) = \begin{cases} \dfrac{1}{C\omega}\left[I_{DC}\theta - I_{RF}\cos(\theta+\varphi) + I_{RF}\cos\varphi\right] + \\ + r_C\left[I_{DC} + I_{RF}\sin(\theta+\varphi)\right] + (I_{DC} + I_{RF}\sin\varphi)r_{on} + \\ + L_{gnd}\omega I_{RF}\cos(\theta+\varphi); \theta\in[0,\pi) \\ \left[I_{DC} + I_{RF}\sin(\theta+\varphi)\right]r_{on} + \\ + L_{gnd}\omega I_{RF}\cos(\theta+\varphi); \theta\in[\pi,2\pi) \end{cases}$$

An excess reactance X (represented by C_x) is added in series with R_L (see figure 3), in order to achieve the correct phase at the load. This reactance together with the load resistance forms an impedance Z:

$$Z = R_L + jX = \sqrt{R_L^2 + X^2}\,e^{j\arctan\frac{X}{R_L}}$$

Since the resonator L_0, C_0 is tuned on the ω frequency, it behaves like a short-circuit for the fundamental component of the v_t voltage and introduces an infinite impedance for the harmonics. In this way, the voltage that drops on the Z impedance is in fact the fundamental component of the v_t voltage. It is therefore necessary to determine through Fourier analysis the amplitude and the phase of this component from the Fourier coefficients V_{Tcos} and V_{Tsin}:

$$V_{T\cos} = -\frac{I_{RF}}{\pi C\omega}\left(2\sin\varphi + 2C\omega r_C\cos\varphi + \frac{\pi}{2}\cos\varphi\right) + \\ + \frac{I_{RF}}{2}(r_C + r_{on})\sin\varphi + I_{RF}L_{gnd}\omega\cos\varphi$$

$$V_{T\sin} = \frac{I_{RF}}{C\omega}\left(\sin\varphi + C\omega r_C\cos\varphi + \frac{1}{2}\sin\varphi + \frac{2}{\pi}\cos\varphi\right) + \\ + \frac{r_C I_{RF}}{\pi}\left(2\sin\varphi + 2C\omega r_C\cos\varphi + \frac{\pi}{2}\cos\varphi\right) + \\ + r_{on}I_{RF}\left(\frac{2}{\pi}\sin\varphi + \frac{1}{2}\cos\varphi\right) - I_{RF}L_{gnd}\omega\sin\varphi$$

The voltage across the switch can now be written as:

$$V_{T1} = \sqrt{V_{Tsin}^2 + V_{Tcos}^2}\,e^{j\psi}$$

where:

$$\tan\psi = \frac{V_{Tcos}}{V_{Tsin}} \qquad (4)$$

As this voltage is applied on the impedance Z, the following current will flow through the load:

$$I_{RF} = \frac{V_{T1}}{Z} = \frac{|V_{T1}|}{\sqrt{R_L^2 + X^2}}e^{j\left(\psi - \arctan\frac{X}{R_L}\right)}$$

But the RF current in this RLC branch must be of the form:

$$I_{RF} = |I_{RF}|\,e^{j\varphi}$$

It now becomes clear the reason why the excess reactance was introduced into the circuit. Since the fundamental component of the v_t voltage has a phase ψ that differs from the φ phase of the current in the RLC branch, this excess reactance X is used to correct the phase at the load.

With these two last complex equations we get:

$$|I_{RF}|e^{j\varphi} = \frac{|V_{T1}|}{\sqrt{R_L^2 + X^2}}e^{j\left(\psi - \arctan\frac{X}{R_L}\right)}$$

The excess reactance X added in series with R_L, in order to achieve the correct phase at the load, must be:

$$X = R_L\tan(\psi - \varphi) \qquad (5)$$

while the amplitude of the RF current is:

$$|I_{RF}| = \sqrt{V_{Tcos}^2 + V_{Tsin}^2} \,/\, \sqrt{R_L^2 + X^2}$$

Combining these equations, we get:

$$R_L = \frac{\sqrt{V_{Tcos}^2 + V_{Tsin}^2}}{I_{RF}\sqrt{1 + \tan^2(\psi - \varphi)}} \qquad (6)$$

The RF current amplitude I_{RF} can be found as:

$$I_{RF} = \sqrt{\frac{2P_{out}}{R_L}} \qquad (7)$$

The average value of v_t must equal V_{DC}, since it is connected to the DC power supply through a RF choke:

$$V_{T0} = \frac{1}{2\pi}\int_0^{2\pi} v_t(\theta)\,d\theta = V_{DC}$$

Please note that the ground inductance voltage has no influence upon this average, since it contains no DC component. Now the shunt capacitor can be calculated from the equation below:

$$2C^2\omega^2\pi r_S r_C\cos\varphi + \frac{\pi^2}{2}\sin\varphi + 2\sin\varphi + \pi\cos\varphi + \\ + C\omega\left[\left(\frac{\pi^2}{2}r_C - 2r_S\right)\cos\varphi + 3\pi r_S\sin\varphi - 2\pi\frac{V_{DC}}{I_{RF}}\right] = 0 \qquad (8)$$

The circuit parameters are calculated through an iterative method, starting with the solution obtained under ideal conditions. The steps to be followed are:

1. φ angle is calculated using the ideal value of C and equation (3).

2. V_{Tcos} and V_{Tsin} are determined using the value of φ from step 1.

3. Based on step 2, the value of ψ is calculated from (4).

4. The load resistance value R_L is obtained from equation (6).

5. The current I_{RF} is computed using (7).

6. Based on the results obtained so far, the second-order equation (8) can be solved and a valid solution for C is retained.

7. Compare the value of C obtained in step 6 with the one used in steps 1-5. If the difference is small enough, it can be considered that the algorithm has converged and step 8 can follow. Otherwise, with the new value of C, go back to step 1.

8. Using the equation (5) calculate the excess reactance X. For the series resonant circuit the equations used for the ideal case are valid.

As simple as it may seem, the numerical treatment of this algorithm is not completely straightforward. In particular, it is hard to distinguish between the regions when there is no solution and those where there is one but the numerical method is divergent. Mathematically, the above problem reduces itself at finding the fixed points of an application of the form:

$$C = f(C, \omega, P_{out}, V_{DC}, r_C, r_{on}, L_{gnd})$$

To be sure there is no fixed point for a given set of input parameters, the entire real axis has to be swept, which is numerically impossible.

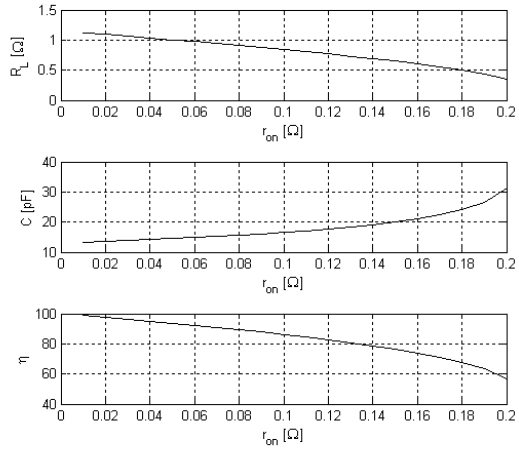

Fig. 4: The influence of r_{on} when r_C=0.

If the algorithm succeeds in providing a solution, the efficiency can be calculated:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{R_L I_{RF}}{2V_{DC}(C\omega r_C \cos\varphi + \sin\varphi)} \qquad (9)$$

The first thing to be noticed after running having run this algorithm for $L_{gnd}\neq 0$ is that a negative value results for the excess reactance X. This indicates that a capacitor instead of an inductor (as used when L_{gnd}=0) has to correct the phase at the load.

An interesting result is obtained for r_{on}=r_C=0: if there are no other losses in the circuit, the efficiency will remain at the theoretical value of 100%. This can be explained through the simple fact that the class-E operation requirements (which guarantee the 100% efficiency) are applied to the switch – shunt capacitor loop, which is not affected by the parasitic ground inductance.

The efficiency drops as r_{on} and r_C is increasing. Also, in order to maintain the class-E operation and to obtain the nominal output power, the load resistance has to be decreased and the shunt capacitor has to be increased.

Comparing the two non-idealities when they occur independent from one another, it results that the losses are caused mainly by r_{on}; the effects of r_C can be neglected. In figure 4, the impact of r_{on} upon the circuit can be seen for the case when r_C=0, f=1.95 GHz, V_{DC}=1 V, P_{out}=0.5 W. Analyzing the efficiency curve, the importance of a small on-resistance becomes clear.

3.2 Effects of the finite turn-off time

As known, for the class-E operation the switch has to close when the current through it is zero, but has to open at a moment when the current has an important value. Since the switch is implemented using a MOS transistor, the drain current cannot drop instantly to zero, thus resulting in power losses during the on-to-off transition.

As shown in (Raab and Sokal, 1978), an estimate for the power loss due to the finite time of transistor's turn-off can be obtained assuming that the current drops down linearly.

Ignoring the effects of the on-resistance of the transistor as well as other losses, the power dissipated due to transistor's switching time is then simply:

$$P_{dtran} = \frac{1}{2\pi}\int_0^{\theta_{off}} v_{Coff}(\theta) i_{swoff}(\theta) d\theta = \frac{i_{open}^2}{48\pi\omega C}\theta_{off}^2 \qquad (10)$$

where i_{open} is the current through the switch at the moment of opening and θ_{off} is the moment when the current is reaching zero value.

3.3 Total power dissipation

The main causes for power dissipation considered in our analysis are:

- the transistor on-resistance
- the shunt capacitor finite Q-factor
- the finite turn-off time

A method to calculate the total power dissipation is to estimate the power losses for each particular cause, neglecting the effect of the others (Raab and Sokal, 1978). The global efficiency will then be:

$$\eta_{tot} = \frac{P_{out}}{P_{out} + P_{dtot}}$$

where P_{out} is the desired output power and P_{dtot} is the total power loss.

The class-E PA global efficiency can be estimated as follows. First, using the algorithm described in Section 3.1, the power loss P_{d12}, due to the transistor on-resistance and the finite value of the shunt capacitor Q-factor, is calculated; $\eta_{1,2}$ is the corresponding efficiency (eq. (9)). Second, the power loss P_{dtran} due to the finite turn-off time (10) is accounted for. The global efficiency becomes:

$$\eta_{tot} = \frac{P_{out}}{P_{out} + P_{d12} + P_{dtran}} = \left(\frac{1}{\eta_{1,2}} + \frac{\sin^2\varphi}{6\pi\omega CR}\theta_{off}^2\right)^{-1} \qquad (11)$$

In the case of a discrete implementation, the algorithm in Section 3.1 would be executed for L_{gnd}=0, resulting the network component's values and an estimate for the efficiency. In order to calculate the total power loss, equation (11) can be applied taking

care to add also the loss due to the switch ground inductance (Raab and Sokal, 1978).

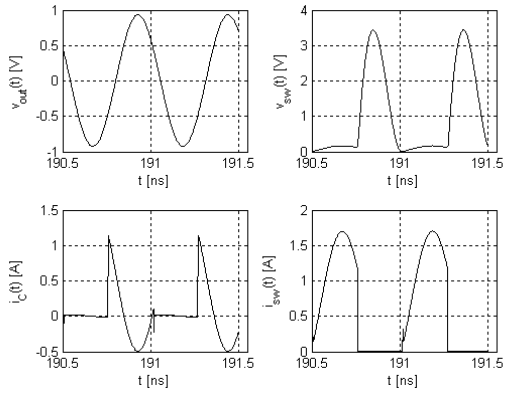

Fig. 5: Voltage and current waveforms of the simulated class-E PA.

4. SIMULATION RESULTS

In order to verify the theory predictions, a class-E PA is designed to meet the UMTS specifications and then simulated using PSPICE. The design frequency corresponds to the centre of the UMTS transmit-band (f=1.95 GHz). The output power is P_{out}=0.5 W (27 dBm). Because an integrated implementation in a standard low-voltage CMOS process is expected, it is assumed that the transistor has a breakdown voltage of only 3.6 V. In order to avoid breakdown, a DC supply voltage of only 1 V is chosen. As we already have shown, the influence of r_C is small and can therefore be neglected. We choose a small but non-zero value r_C=0.01 mΩ, while r_{on}=100 mΩ and L_{gnd}=0.2 nH. The simulation will not take into account a finite turn-off time. The values of the passive network, the currents and voltages calculated by the algorithm described in Section 3.1 are:

$R_L = 0.84\,\Omega$	$C = 16.5\,\mathrm{pF}$
$L_0 = 6.86\,\mathrm{nH}$	$C_X = 53.69\,\mathrm{pF}$
$C_0 = 971.35\,\mathrm{fF}$	$I_{RF} = 1.09\,\mathrm{A}$
$I_{DC} = 0.58\,\mathrm{A}$	$I_{pk} = 1.67\,\mathrm{A}$
$\varphi = 2.581\,\mathrm{rad}$	$\eta = 86.1\%$

After tuning the circuit slightly, as described in (Sokal, 2001), the PSPICE simulation offers the following results:

$C = 15\,\mathrm{pF}$	$C_X = 52\,\mathrm{pF}$
$I_{RF} = 1.11\,\mathrm{A}$	$I_{DC} = 0.61\,\mathrm{A}$
$I_{pk} = 1.72\,\mathrm{A}$	$P_{out} = 0.518\,\mathrm{W}$
$\eta = 84.8\%$	$V_{pk} = 3.44\,\mathrm{V}$

As it can be seen, the values obtained by simulation are very close to the calculated ones, thus proving the validity of the design method. The voltage and current waveforms are plotted in figure 5.

5. CONCLUSIONS

A new class-E PA design methodology has been presented. An iterative algorithm for determining the class-E network elements, when switch- and shunt capacitor-losses and a parasitic ground inductance are simultaneously present, has been developed. The total power dissipation was calculated considering also the effects of the finite turn-off time. It has been shown that the circuit can be designed to function even with a large value for the parasitic ground inductance, although the frequency is situated in the microwave range. The simulations have confirmed the theoretical results.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the useful comments and discussions had with Prof. Dr. Kurt Hoffmann, Dr. Rainer Kraus and Jiawen Hu and thank the stuff of the Institute for Electronics, University of the Federal Armed Forces, Munich, for their support while the work was carried out.

REFERENCES

Cripps, S. (1999). *RF Power Amplifiers for Wireless Communication*. Artech House.

Hella, M. and M. Ismail (2002). *RF CMOS Power Amplifiers: Theory, Design and Implementation*. Kluwer Academic Publishers.

Kazimierczuk, M. K. and K. Puczko (Feb. 1987). Exact Analysis of Class E Tuned Power Amplifier at any Q and Switch Duty Cycle. *IEEE Transactions on Circuits and Systems*, **vol. CAS-34, No. 2**.

Milosevic, D., J. van der Tang, A. van Roermund. Analysis of Losses in non-ideal passive Components in the Class-E Power Amplifier. *http://zeus.ics.ele.tue.nl/~dmilosev/*

Raab, F. H. and N. O. Sokal (Dec. 1978). Transistor Power Losses in the Class E Tuned Power Amplifier. *IEEE J. Solid-State Circuits*, **vol. SC-13, No. 6**.

Sokal, N. O. (2001). Class-E RF Power Amplifiers. *http://www2.arrl.org/tis/info/pdf/... ...010102qex009.pdf*

Zulinski, R. E. and J. W. Steadman (Sept. 1987). Class-E Power Amplifiers and Frequency Multipliers with Finite DC-Feed Inductance. *IEEE Transactions on Circuits and Systems*, **vol. CAS-34, No. 9**.