A CMOS LOW VOLTAGE CLASS-E POWER AMPLIFIER FOR UMTS

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Abstract: In this paper we design a low-voltage class-E power amplifier (PA) in a standard CMOS 0.35µm integrated technology, to be used in a UMTS transceiver having the following specifications: f=1.95 GHz, V_{DC}=1 V, P_{out}=0.5 W. The designed class-E network accommodates the simultaneous presence of a parasitic ground inductance and losses in the switch and shunt-capacitor. The transistor is dimensioned for an optimum PAE (power added efficiency). Finally, we simulate the power control capabilities and highlight linearization methods.

Keywords: Communication Systems, RF Power Amplifiers, Class-E, CMOS

1. INTRODUCTION

The class-E PA is a switching-mode amplifier which could provide, under ideal conditions, 100% efficiency. At low frequencies, a MOS transistor could easily model the ideal switch. Above this frequency range the effects of both transistor's switching time (which becomes a significant percentage of the RF cycle) and the device parasitics become important, therefore decreasing the amplifier's efficiency.

In the context of the "System-on Chip" concept (Negut *et al*., 2005; Hella and Ismail, 2002), the design of the power amplifier is not an easy task, because at a first glance the CMOS component menu would seem unsuitable. Indeed, CMOS transistors have low breakdown voltage, can achieve only low gain and due to substrate coupling different stages can disturb each other. In addition, improved high frequency MOS devices models are needed to simulate accurately the power amplifier which is a large signal circuit. Another important issue is the power dissipation, which must not be excessive, although a power amplifier handles large currents. In this context, high efficiency is a must.

Despite these obstacles, practical implementations of CMOS class-E power amplifiers have been reported, thus proving the feasibility of the project (Hella and Ismail, 2002; Tsai and Gray, 1999; Ho and Luong, 2003; Tan *et al.*, 2000).

Nonlinearity is a major disadvantage of the class-E PA. It would seem that only frequency and phase modulated signals are suited for this type of amplifier (as used in GSM), but with a proper linearization technique, also amplitude modulated signals can be successfully amplified. The UMTS standard uses a WCDMA (Wideband Code Division Multiple Access) radio interface and a QPSK (Quadrature Phase Shift Keying) modulation scheme. The resulted signal has non-constant envelope, so the class-E PA must be linearized in some way (Milosevic, 2003). One method which proved to be feasible is EER (*Envelope Elimination and Restoration*): since the output power is a linear function of power supply voltage V_{DC}, the output is remodulated by modulating the supply voltage with the signal envelope. Of course, the linearization circuit needs to be linear and power efficient, in order not to degrade the overall efficiency.

Another disadvantage is the high value of the peak voltage on the transistor. For a class-E design, technologies with high breakdown voltage are required, but high-speed CMOS-integrated devices have low breakdown voltage. In this case, the only solution is to lower the supply voltage, but this will result in further decrease of the load resistance, thus making the impedance transformation to 50 Ω more difficult.

The paper is structured as follows: Chapter 2 evaluates the parasitics of the MOS transistor as they result from the layout. In Chapter 3 the transistor is dimensioned, the class-E network is calculated and a trimming is performed based on simulation results. Chapter 4 investigates the output power controllability and the possibilities for linearization. In Chapter 5 the conclusions are summarized.

2. LAYOUT CONSIDERATIONS

Since the whole design performance is mainly determined by the MOS transistor operation as a switch, an estimate of its characteristics is a must. The parasitics of the active device are a function of the transistor's layout. Using the 0.35 µm DRC values and the electrical parameters provided by the foundry, an estimate of the physical dimensions of the device and parasitics will be obtained. The transistor will be drawn in an interdigitated structure, each finger having L=0.35 µm and W=20 µm.

The ideal switch is replaced by the equivalent circuit of a MOS device, as shown in figure 1. R_S, R_D and R_G include the parasitic resistances, such as ohmic contact resistances, leads, bond wires. Besides this, R_G includes the polysilicon sheet resistance too, modelled as a distributed RC network.

Since most of the junctions are shared between two consecutive transistors, care must be taken when calculating the parasitic capacitances. Because of the transistor dimensions, it is very difficult to estimate accurately the effects of the gate-to-channel and channel-to-substrate capacitances, since they should be rather modelled as distributed RC networks. For hand analysis, simplified models can be used as shown in (Johns and Martin, 1997).

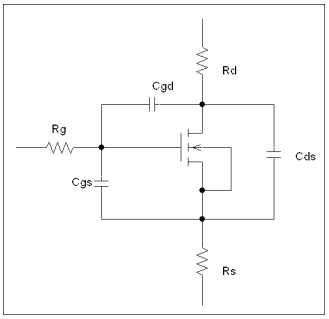

Fig. 1: MOS equivalent circuit (simplified).

The capacitances shown in figure 1 must be calculated separately for triode and cut-off regions and they usually depend on the bias conditions. The total capacitance of the device can be found by multiplying the capacitance of one finger with the total number of fingers. It should be noted that such a hand-analysis provides the worst case estimate for the parasitics.

Another important issue is the effect of bonding wires parasitic inductance. Using typical values provided by the foundry (AMS, 1998), it is found that every bond wire has an inductance of about 1 nH (figure 2). The coupling factor between two adjacent bond-wires is about K=0.3, while the coupling factor between the non-adjacent ones is K'=0.2. Every bond wire has an ohmic resistance of about 50 mΩ and the pads where they are attached have a capacitance of about 170 fF. As a consequence of the mutual couplings, the connection of m bond wires in parallel will not result in a decrease of the total inductance by the same m factor. The model is simulated in Cadence SpectreRF and a number of 8 parallel connected bond wires is chosen, as a trade-off between the parasitic ground inductance value and the necessary number of bond wires. The equivalent ground connection at the operating frequency is shown in figure 3.

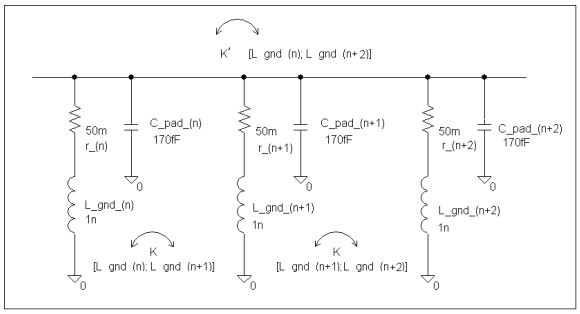

Fig. 2: Mutual couplings between bond-wires.

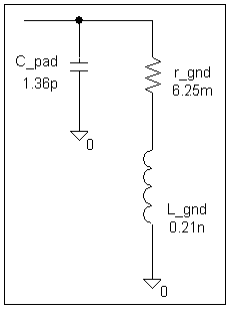

Fig. 3: Equivalent circuit of the ground connection at the operating frequency.

3. DIMENSIONING THE TRANSISTOR. FINE TUNING OF THE CLASS-E DESIGN

The MOS transistor size has to be next established, so that the device can support the needed current and provide a low on-resistance. Conflicting requirements have to be dealt with, since the power needed

to drive the MOS transistor is increasing with the frequency due to the input capacitance, which is a function of the transistor's size.

As was shown in (Negut *et al.*, 2005) the transistor have to be designed as wide as possible in order to get the smallest on-resistance value. In this way the transistor input capacitance becomes larger and the power added efficiency (PAE),

$$PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}},$$

decreases due to larger input power required to drive the stage.

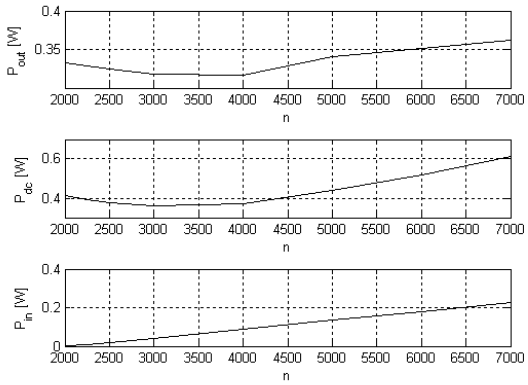

Fig. 4: Amplifier's output, DC and input power versus the number of fingers.

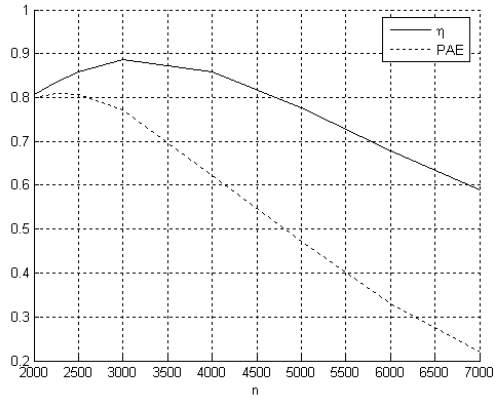

Fig. 5: Efficiency and PAE versus the number of fingers.

A first order estimate for the number of transistor's fingers will be made using the classic MOS equation for the triode region:

$$i_{\text{D}} = \mu_{\text{n}} C_{\text{ox}} \frac{W}{L}\left[(v_{\text{GS}} - V_{\text{th}})v_{\text{DS}} - \frac{v_{\text{DS}}^2}{2}\right] \qquad (1)$$

Since equation (1) provides only a simple model for the MOS transistor, an equivalent value for $\mu_{\text{n}}C_{\text{ox}}$ is obtained through simulations using the more complex and realistic BSIM3v3 device model. If we consider that the gate-to-source voltage is constant during conduction and we neglect the v_{DS}^2 term in (1) due to its small enough value, a constant drain-to-source resistance results:

$$r_{\text{DS}} = \left[\mu_{\text{n}} C_{\text{ox}} \frac{nW}{L}(v_{\text{GS}} - V_{\text{th}})\right]^{-1}$$

where W is the width of one finger.

The diffusion sheet resistance of the drain/source area (R_{sheet}), the spreading resistance which arises from the current spreading from the channel (R_{spread}) and the accumulation layer resistance (R_{accum}) are also important for deep submicron MOS devices. Adding also the ohmic contact resistances due to diffusion contacts and via contacts, the final on-resistance of the MOS is obtained:

$$r_{on} = \left[\mu_{\text{n}} C_{\text{ox}} \frac{nW}{L}(v_{\text{GS}} - V_{\text{th}})\right]^{-1} + \frac{R_{\text{DSsa}}}{n} + \frac{r_{\text{cont}}}{n} \qquad (2)$$

Accepting a power loss corresponding to an efficiency of about 86%, an on-resistance of 100 mΩ results. This value of efficiency is considered to be acceptable, since smaller on-resistances can be obtained only by severe increase of the transistor's size. In fact, for a too large transistor, the parasitics would be so large, that the output capacitance would be larger than the needed shunt capacitor and the PAE would be extremely low (as the input power would be considerable). Introducing the previous determined on-resistance in equation (2), a number of necessary fingers is obtained:

$$n = 3858.$$

The class-E network will be designed using the algorithm described in (Negut *et al.*, 2005). As we already showed, the influence of r_{C} is small and can therefore be neglected. We choose a small but non-zero value r_{C}=0.01 mΩ, while r_{on}=100 mΩ. In order to avoid the breakdown of the device, a 1 V DC-supply is used. The values of the passive network, the currents and voltages calculated by the algorithm are:

$R_{\text{L}} = 0.84\,\Omega$	$C = 16.5\,\text{pF}$
$L_0 = 6.86\,\text{nH}$	$C_{\text{X}} = 53.69\,\text{pF}$
$C_0 = 971.35\,\text{fF}$	$I_{\text{RF}} = 1.09\,\text{A}$
$I_{\text{DC}} = 0.58\,\text{A}$	$I_{\text{pk}} = 1.67\,\text{A}$
$\varphi = 2.581\,\text{rad}$	$\eta = 86.1\%$

Adding the effects of the finite turn-off time of the transistor, the efficiency becomes:

$$\eta_{\text{tot}} = 85.3\,\%.$$

As it can be seen, although a large parasitic ground inductance is present, the efficiency has a quite large value, because the used algorithm accommodates the effects of the ground inductance.

Simulating the designed circuit, a sweep of the number of fingers will be next performed and the maximum PAE will be sought. An analytical approach for the calculation of the input power was avoided, since the results given by the simplified model used in hand-analysis proved to have little to do with the results offered by SpectreRF using BSIM3v3 models.

A squarewave signal should be used for transistor driving, but this would be very difficult at high frequency. Instead, a sinusoidal wave with an appropriate offset is used. The bias voltage for the gate was

chosen equal to the threshold voltage (about 0.5 V) in order to have 50% duty cycle. The amplitude of the input was considered to be 1 V. Because a large transistor is expected, *no external shunt capacitor is used*, so that the output parasitics of the transistor must provide the entire needed capacitance.

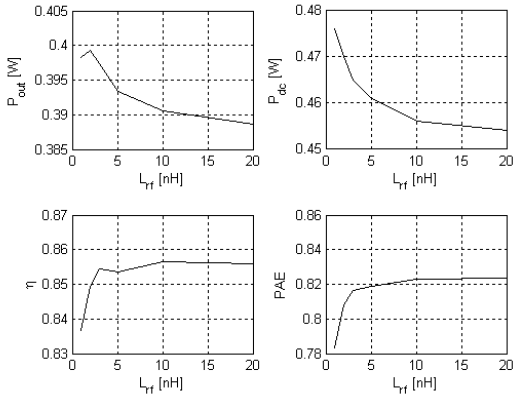

Fig. 6: Output power, DC power, efficiency and PAE versus the DC feed.

The simulated characteristics of the class-E amplifier are plotted in figures 4 and 5 versus the number of fingers. Results for n<2000 are not considered, since the transistor is too small to support the needed current. As it can be seen, output power is slowly increasing with n, while the input power is rapidly increasing. As a normal consequence, the gain and PAE exhibit peak values. From the system design point of view, PAE is the most important figure of merit and the optimization will be made in order to maximize its value.

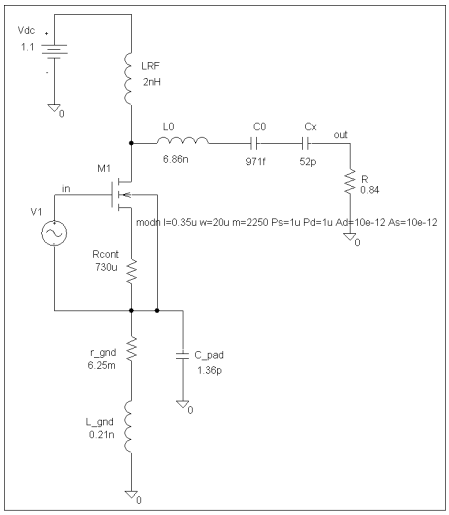

Fig. 7: Tuned class-E power amplifier.

Choosing n=2250 (where PAE is maximum), the circuit needs further "trimming", since the voltage and current waveforms indicate that the class-E operation conditions are not completely met. First of all, a convenient excess capacitance is being sought; next, the bias voltage is being varied, in order to maximise the *PAE*. At last, the amplitude of the input voltage is being swept. It must be noted that any change of the bias voltage or amplitude of the input voltage will also result in a duty cycle change. Because the shunt capacitance is larger than optimum (due to the output parasitics of the active device) and the optimization was made for maximum PAE, the output power is smaller than desired (only 25.9 dBm).

An interesting issue is the RF choke value. In (Zulinski and Steadman, 1987) it is shown that the class-E amplifiers can provide greater output power when a finite DC feed is used and can accommodate arbitrary output capacitance. From figure 6 it can be seen that for our particular design no important increase in output power is obtained when decreasing the DC feed. Nevertheless, the possibility of avoiding the RF choke without sacrificing the efficiency (as seen in figure 6) brings considerable advantages. In the first place, a smaller DC feed inductance can be easily integrated, for example by using bond wires (small series resistance is needed, since the supply current is large enough). Second, the DC feed must permit the entire spectrum of the input-signal envelope to pass through (Milosevic, 2003), if the EER technique will be used for linearization.

After choosing a 2 nH value for the DC feed inductance and the output power is increased through the adjustment of the DC supply voltage (1.1 V instead of 1 V), the final solution is (see figure 7):

N=2250	R=0.84 Ω
L_0=6.86 nH	L_{rf}=2 nH
C_0=971 fF	V_{bias}=0.7 V
C_x=52 pF	V_{in}=0.9 V

corresponding to the following performances:

$$PAE = 81.8\%$$
$$\eta = 84.8\%$$
$$P_{out} = 0.483\,\mathrm{W}$$
$$G = 14.5\,\mathrm{dB}$$

The efficiency obtained from the simulations is very close to the one predicted by theory. In figure 8, the drain-to-source and output voltages from the SpectreRF transient simulation are plotted. It can be seen that the class-E conditions are sufficiently well met.

4. OUTPUT POWER CONTROLLABILITY

Next the issue of the output power controllability will be analysed. Theoretically, the output power is proportional to V_{DC}^2, thus allowing for linearization techniques to be applied.

As it can be seen from figure 9, the output power versus power supply voltage can be approximated by a parabolic function:

$$P_{out}(V_{DC}) = 0.3984V_{DC}^2 - 0.00608V_{DC} + 0.006741 .$$

This behaviour is due to the complex phenomena occurring during the operation of the MOS device.

Nevertheless, efficiency displays a remarkable feature: in the 0.3…1.3 V range it is almost constant with the supply voltage. This implies that a linearization technique as *Envelope Elimination and Restoration (EER)* is worth to be implemented, although the characteristic $P_{out}=f(V_{DC})$ has to be dealt with and a form of compensation must be used. It should be reminded that conventional power amplifiers have optimum efficiency only for maximum output power, so that, since the power is fluctuating due to amplitude modulation, in average the amplifier actually works with a lower efficiency. Class-E is not suffering from this issue.

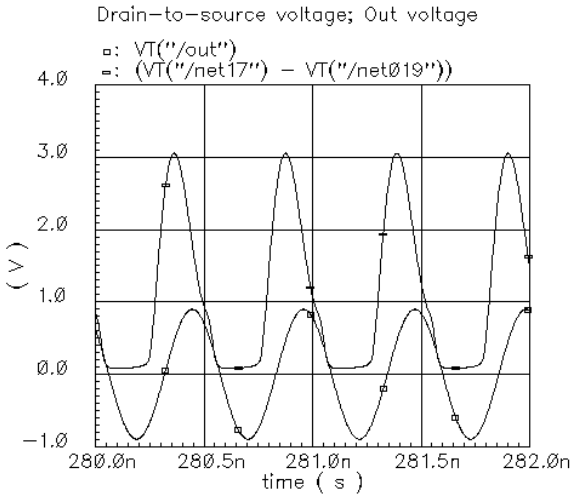

Fig. 8: Drain-to-source and output voltages.

For V_{DC}<0.3 V the efficiency seems to be bigger than unity. More, *PAE* becomes negative, which shows that more power is injected into the circuit than it is extracted. The reason for this behaviour is that the input power is transferred to the output through the feed-back loops existing in the circuit due to parasitics. Also, simulation errors are suspected. Due to this behaviour, the operation below 0.3 V should be avoided.

5. CONCLUSIONS

A CMOS class-E power amplifier design methodology has been presented and it has been shown that a low-voltage implementation for UMTS is possible.

The class-E network elements values were determined using an iterative algorithm which accommodates simultaneously the losses in the switch and shunt capacitor, together with the parasitic ground inductance. The total power dissipation was calculated considering also the effects of the finite turn-off time.

After the transistor has been dimensioned for maximum *PAE*, a fine tuning of the circuit and simulations revealed that the performance is within expectations, displaying high efficiency. Since the output power was smaller than desired, the supply voltage was little increased. The efficiency is bigger than the one that could be obtained with a conventional amplifier, so the design is well suited for mobile applications. Another advantage is also the fact that all the needed shunt capacitance is provided by the transistor's output capacitance, thus saving die area. The RF choke was replaced by a small DC feed inductance, easy to be integrated.

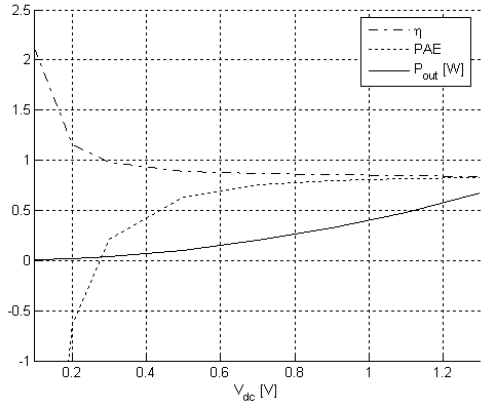

Fig. 9: Output power and efficiency versus the supply voltage (simulation result).

The possibilities for EER linearization technique have been proven, since the amplifier exhibits almost constant efficiency with power supply and the output power follows a parabolic curve which can be compensated by the linearization circuit.

The matching network necessary for the circuit's output has not been discussed here, but it should be implemented off-chip, in order to have a sufficient high quality factor and to be able to support the output current. A driver stage capable of driving the big capacitive load represented by the PA must be placed at the input and must share the same ground connection (see figure 7, where the generator is connected directly between the gate and the source). Any other needed matching networks can be implemented on-chip, since the current involved has a smaller value.

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