ASIC BASED DESIGNS FOR ENERGY METERS

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Abstract: The paper presents some of the practical problems issued by the design of the energy meters, focusing on the chips provided by Analog Devices Inc (ADI).
Aspects of the power and energy digital measurement are considered. An experimental model of an energy meter and power quality monitor is also described.

Keywords: Energy Meter, Digital Monitor, Power Measurement

1. INTRODUCTION

Electromechanical meters were the first standard energy measuring equipment since electricity billing started. Today's electricity companies are demanding more information from meters in the residential sector, where metering has typically been limited to kilowatt-hours. New features such as multi-tariff billing, reactive energy measurement and power quality monitoring are desirable to improve generation, distribution, customer service and billing.
In order to accommodate the advanced requirements not available in electromechanical meters, manufacturers have begun adopting all-electronic solutions. New energy measurement ASIC (Application Specific Integrated Circuits) are enabling accurate, dependable and robust meters.
In the field of digital measurements, the energy meters and power quality monitors became a necessity because there are more and more nonlinear loads due to the extended use of the switch mode power supplies and power controllers and invertors.
The old energy measurement equipment becomes obsolete and needs to be replaced with modern digital meters. Most of the ASIC offer a wide range of additional features along with the power and energy metering features.
A study was developed in order to design energy meters meeting well known conditions: high performances and low price. We concluded ADI chips seem to be the best choice, gathering together the high precision, the high reliability of the new technology at acceptable price.

2. MAIN FEATURES

Two main categories of energy metering ASIC are on the specific market from ADI Corporation (Analog Devices, Inc. - Energy Measurement IC and System Solutions): pulse output ASIC (ADE7751, ADE7755, ADE7757, ADE7757a, ADE7768, ADE7769, ADE7760, ADE7761 and ADE7752) and SPI output ASIC (ADE7753, ADE7756, ADE7759, ADE7763, ADE7754 and ADE7758), for single phased applications (ADE7751, ADE7755, ADE7757, ADE7757a, ADE7768, ADE7769, ADE7760, ADE7761, ADE7753, ADE7756, ADE7759 and ADE7763) and three phased applications (ADE7752, ADE7754 and ADE7758).
The analog interface for the current inputs of these circuits may be represented by micro-ohm resistive shunts (all), current transformers (all), hall sensor current transducers (all) or Rogowski coil current transducers (ADE7753, ADE7759, ADE7763 and ADE7758). Key features of these ASICs refer to:
- active energy metering (all);
- reactive energy metering (ADE7753, ADE7758);
- aparent power and energy metering (ADE7753, ADE7763, ADE7754 and ADE7758);
- hardware (pulse output chips) and software (SPI chips) calibration;

- reverse power indication (ADE7755, ADE7757a, ADE7768, ADE7769 and ADE7752);
- fault tolerant billing (ADE7751, ADE7760, ADE7761 and ADE7752);
- missing neutral billing (ADE7761).

Additional features are provided for the power quality metering:
- RMS calculation for current and voltage channels (ADE7753, ADE7763, ADE7754 and ADE7758);
- zero crossing logic output (ADE7753, ADE7756, ADE7759, ADE7763, ADE7754 and ADE7758);
- sag detection (ADE7756, ADE7758);
- current / voltage peak values detection (ADE7758);
- no load detection (ADE7758 and ADE7769);
- serial port and interrupt (ADE7753, ADE7756, ADE7759, ADE7763, ADE7754 and ADE7758)
- power quality supervisory (ADE7753, ADE7756, ADE7759, ADE7763, ADE7754 and ADE7758);

Most of the ASICs mentioned above include on-chip oscillator for the main clock signal.

The only chip that accumulates only the positive power flow is ADE7768. All other chips include bidirectional power flow counters.

3. DESIGN CONSIDERATIONS

3.1. Accuracy Considerations

The International Standard IEC 61036 (2000-09), Alternating Current Static Watt-Hour Meters for Active Energy (Classes 1 and 2), are used as the primary specification for energy meters designs, as the ANSI C12.16 specifications. The IEC 61036 key specifications in terms of their ANSI equivalents are explained below. IEC 687 – second edition is also applied in the new energy meters' design.

The chips dedicated to three phased circuits energy measurements comply with the IEC 60687, IEC 61036, IEC 61268, IEC 62053-21, IEC 62053-22, and IEC 62053-23 international standards.

Table 1. Error limits for different current ranges

Current Value	PF	Error Limits Class 1	Class 2
0.05Ib…0.1Ib	1	1.5%	2.5%
0.1Ib…Imax	1	1%	2%
0.1Ib…0.2Ib	0.5 lag	1.5%	2.5%
	0.8 lead	1.5%	2.5%
0.2Ib…Imax	0.5 lag	1%	2%
	0.8 lead	1%	2%

The current ranges for specified accuracy shown in Table 1 are expressed in terms of the basic current (Ib). The basic current is defined in IEC 61036 (2000–09) Section 3.5.1.1 as the value of current in accordance with which the relevant performance of a direct connection meter is fixed. I_{MAX} is the maximum current at which accuracy is maintained. Typical values for I_{MAX} are 4 to 6 times Ib. Power factor in Table 1 can be defined as PF =cos(φ), where φ is the phase angle between pure sinusoidal current and voltage.

Accuracy class index is defined in IEC 61036 (2000–9) Section 3.5.5, page 27, as the limits of the allowed percentage error. The percentage error is defined as:

$$\varepsilon_W^{\%} = \frac{Wm - Wt}{Wt} 100 \qquad (1)$$

where Wm represents the measured energy indicated by the meter and Wt represents the true energy or the reference energy calculated or measured with most precise reference instrumentation.

Table 2 presents accuracy requirements for a 100A single phase watt-hour meter.

Table 2. Accuracy Requirements for 100A Active Energy Meters

Current Value	Power Factor	Percentage Error Limits Class 1	Class 0.5	Class 0.2
0.1Iref-Imax	1	±1%	±0.5	±0.2%
1A	1	±2%	±1%	±0.4%
3A	0.5 lag	±2%	±1%	±0.5%
50A	0.5 lag	±2%	±0.6%	±0.3%
100A	0.5 lag	±2%	±0.6%	±0.3%

3.2. Quadrant Convention

Figure 1 shows the quadrant convention used by the chipset. Import means delivered from the utility to the user, export means delivered by the user to the utility and total means total of all three phases.

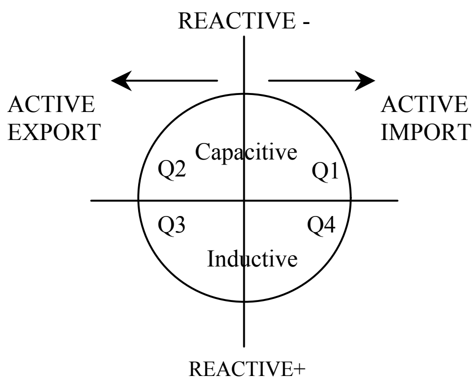

Figure 1. Quadrant Convention

4. HARDWARE CONSIDERATIONS

A common feature of the ADI energy metering ASIC is that the A/D conversion is performed at the channels inputs. The analog circuitry include ADCs and reference circuit only. All the data processing of the main signals is performed in the digital form.

Generally, all energy meters using ASIC include:
- Front end circuitry (interface to the power circuit);
- ASIC that performs all signal processing needed by the RMS, power and energy measurements;

- MCU that controls all the data flow between the ASIC and the user interface;
- Local display and keyboard (user interface), along with a smart menu and a powerful set of soft keys;
- SPI (serial port interface) to communicate with the next level equipment as a RTU or a monitoring PC.

The user may calibrate the gain and/or compensate offset and phase error on every channel of the meter.

4.1. Internal architectures

Figure 2 represents the internal architecture of the ADE7751 energy metering ASIC.

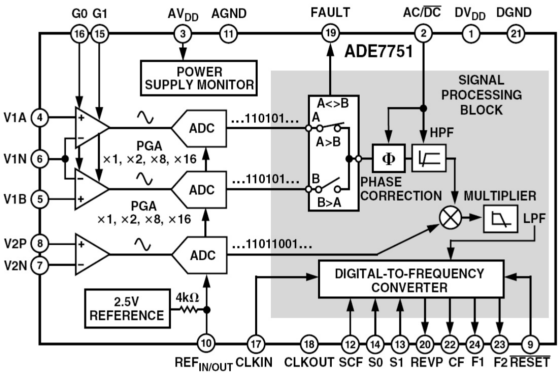

Figure 2. Internal Architecture of ADE7751

The Programmable Gain Amplifier in the input stage, allows the necessary adjustment to achieve the specified dynamic range. A/D Converters perform the digital conversion of all the input signals, allowing the phase correction using simple shifting registers. The digital multiplier performs the power calculation for the digital-to-frequency converter.

The internal architecture of the newest three phased energy meter ASIC (ADE7758) is in figure 3.

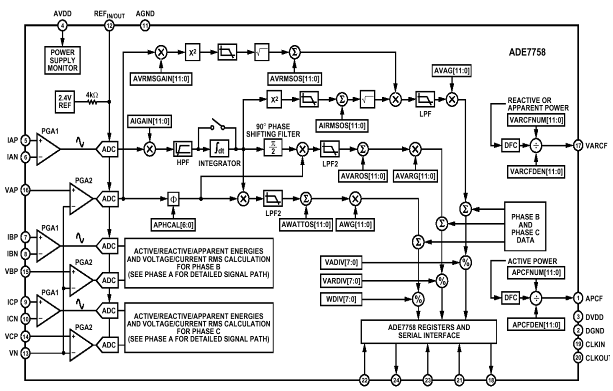

Figure 3. Internal Structure of ADE 7758

One can remark the serial interface and the two pulse outputs. ADE7758 incorporates second-order Σ–Δ ADCs, a digital integrator, reference circuitry, temperature sensor, and all the signal processing required to perform active, reactive, and apparent energy measurement and RMS calculations.

The ADE7758 is able to measure active, reactive, and apparent energy in DELTA or WYE circuits with three or four wires, providing system calibration features for each phase, i.e. RMS offset correction, phase calibration, and power calibration.

5. APPLICATIONS

5.1. Single phase meters

Figure 4 shows an example of a standalone application using the Analog Devices' ADSST-EM-1011 chipset to a highly accurate and low cost Single Phase Electronic Energy Meter of Class 1 accuracy as per IEC61036 or ANSI C12.1 standards. The ADSST-EM-1011 chipset consists of a micro-controller with built-in multi-channel A/D converter, non-volatile memory and UART COM port (Analog Devices, Inc. - ADSST-EM-1010).

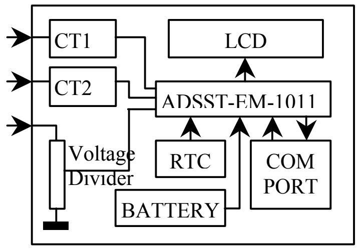

Figure 4. Single Phase Watt-Hour Meter Block Diagram

The phase voltage is scaled down by a resistor network and then passed through a buffer stage. The current signals are sensed by current transformers and are amplified. These conditioned signals are then fed to the ADC channel of the ADSST-EM-1010 for additional processing. From the digitized values of voltage and current, the RMS value of voltage, the RMS value of current, frequency, power factor, and active power are calculated over synchronous intervals. The ADSST-EM-1010 computes the energy by integrating these power measurements. The computed active energy is stored in the internal data memory of the processor. These parameters are cyclically displayed on the 8-digit LCD display.

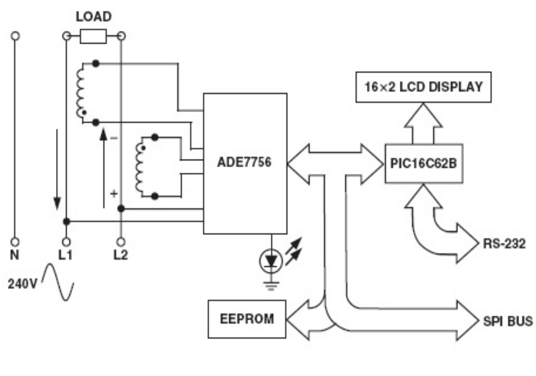

Figure 5. Single Phase Energy Meter with Two CTs

The design offers many features such as measuring active energy, RMS values of the load voltage and current, frequency and power factor measurement, including software based phase and nonlinearity compensation for the current transformers. Two current transformers are used for tamper detection (fig.5). Flags are used to indicate tamper conditions.
An EEPROM is used to store various calibration parameters of the meter and store the meter's data during power-down. The entire meter is calibrated using an external calibration routine and a PC through SPI. Figure 6 represents a practical implementation of a stand alone pulse output watt-hour meter using ADE7757.

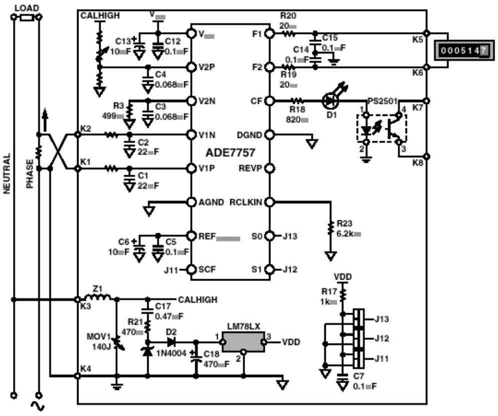

Figure 6. Single Phase Energy Meter Using ADE7757

5.2. Three Phased Energy Meters

The meter in figure 7 (Analog Devices, Inc. - ADSST-EM-2010) supports IEC 60687/61036 and ANSI C12.1/12.20 specifications, meeting Class 0.5 and Class 0.2 full four quadrant energy flow measurement requirements. Pulse output with programmable pulse constant as pulses/kWh or Wh/pulse and programmable duty cycle is available.

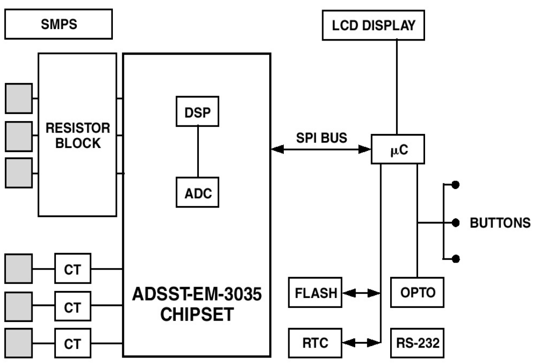

Figure 7. Three Phase Energy Meter Architecture

Gain calibration and DC offset calibration are achieved by embedded calibration routines. Phase and nonlinearity of the current transformers are compensated by software techniques. Tamper conditions are detected and indicated by flags.

Harmonic analysis computes magnitude and phase information for all odd harmonics up to 21st order for all voltage and current channels.
Figure 8 represents the basic block diagram of a signal processing module of a three phased energy meter with power quality analysing functions based on ADE7758 - the latest release of ADI energy metering ASICs (Analog Devices, Inc. - Evaluation Board Documentation ADE7758). The meter was built using the ADE7758 energy metering chip from Analog Devices Inc. The current and voltage transducers may be Hall or Rogowski models, keeping in mind that ADE7758 includes built in integrators on each phase (Analog Devices Inc. - Poli Phase Multifunction Energy Metering IC).
The processed energy data is transferred to the microcontroller or to the PC parallel port through the SPI circuitry, using some combinational circuits to re-shape all digital signals. The digital signals' path include opto-couplers providing complete insulation for the metering section. All security conditions for the human operator and for the computerized instrumentation are accomplished. The power supply have also separate sections in order to provide the same insulation requirements.

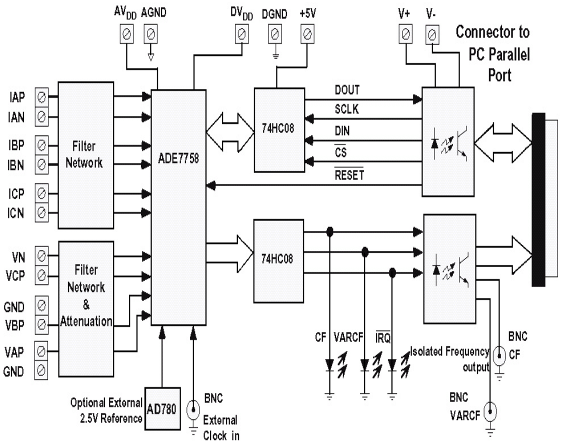

Figure 8. Three Phase Energy Meter with ADE7758

5.3. Dynamic Ranges

All pulse output energy metering ASIC have a dynamic range of 500:1 for the specified precision (0.1%). All SPI out energy metering ASIC have a dynamic range of 1000:1 for the same specified precision (0.1%). The main frequency ranges between 45Hz and 65Hz.

6. SPECIFIC FUNCTIONS

Energy metering ASICs include internal reference circuitry providing the reference voltage for the A/D conversion and power supply monitor (power manager) to protect the data in case of accidental power down.
Two frequency outputs are used to control the output energy counter and to calibrate the meter: the low frequency output is used to drive a two phase stepper

and the high frequency output is used to calibrate the instrument via an optical coupler (Analog Devices - AN679). The hardware design of a SPI ASICs based energy meter must take into consideration the facility of the reading, knowing that the displayed decimal values represent non scaled values of the signals.
Hardware and software adjustments are available. The first allows immediate and very efficient gain adjustments using trimming resistors in all input channels, but no offset compensation. The software allows offset error correction and gain adjustment.

6.1. Tamper detection

One of the optional features is tamper-proof energy metering. If this option is enabled (factory set), the energy meter will function normally even when tampered by one of the three basic tampering methods, including earth tampering. The tampering event is stored in the internal non-volatile memory and the indication can be reset only with an external terminal after verification of password. Figure 9 shows the internal connection of the meter.

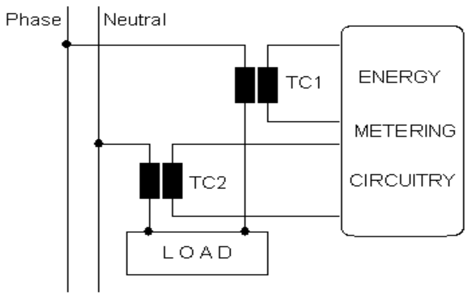

Figure 9. Internal Connection for Tampering Detection

ADI energy metering ASICs incorporate novel fault detection schemes that warn of fault conditions and allow the chips to continue accurate billing during a fault event. The principle of the single phase circuits is monitoring both the phase and the neutral currents. A fault is indicated when these currents differ by more than 12,5% and metering is continued using the larger of the two currents.

7. ADDITIONAL FUNCTIONS

7.1. RMS Calculation

Root mean square (RMS) is a fundamental of the magnitude of an ac signal. Its definition can be both practical and mathematical. Defined practically, the RMS value assigned to an ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Defined mathematically, the RMS value of a sampled signal V(t) is:

$$V_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} V^2(i)} \qquad (2)$$

Figure 10 shows the algorithm implemented for the RMS calculation using samples of the input waveform by means of the signal path in the energy metering chips (Moulin E - RMS Calculation for Energy Meter Applications). The absolute value of the twos complement input is taken first to reduce the number of bits involved. Because the signal is squared afterwards, this block does not affect the final results.

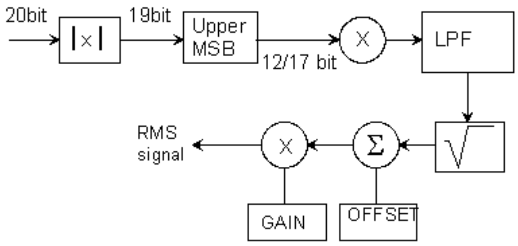

Figure 10. RMS Calculation Signal Path

The upper 12 bit of the voltage channel and 17 bit of the current channel are then extracted to be used in the RMS algorithm. The signal is then squared and low-pass filtered to extract the dc component (figure 1). After the low-pass filter is settled down, the square root is taken and an offset compensation applied. Gain compensation and conversion to true RMS information is then applied to enable the display of the actual value on an LCD display.

7.2. RMS Calculation Errors Compensation

The expected outcome of an RMS calculation is unbiased and stable information. Because signals and signal processing are not ideal, the calculation may be affected by the offset in the input signal and the ripple effect of the multiplication.
A sine wave signal with a small offset:

$$V(t) = V_{os} + V\cos(\omega t) \qquad (3)$$

after the square operation yields to:

$$V^2(t) = V_{os}^2 + \frac{V^2}{2} + 2\,V_{os}V\,\mathbf{cos}\,\omega t + \frac{V^2}{2}\mathbf{cos}\,2\omega t \qquad (4)$$

If the averaging is too short, ripples with ω and 2ω frequencies affect the RMS calculation. A low-pass filter after the square function eliminates this ripple frequency noise. The cutoff frequency of the filter should be low enough to attenuate the ripple frequency by at least 40 dB (Figure 11).
For errors lower than 0.1%, more than 3540 samples are needed, taken over 2.03 seconds at the given sampling frequency. The corresponding error affecting the RMS calculated values is given by:

$$Error(\%) = \frac{100}{\left(1+2^{-9}\right)^n} \qquad (5)$$

where n represents the number of samples.

The offset effect on the RMS calculation is canceled by calibrating the offset error of the measurement and assuming that the offset is a constant variable in the signal processing.

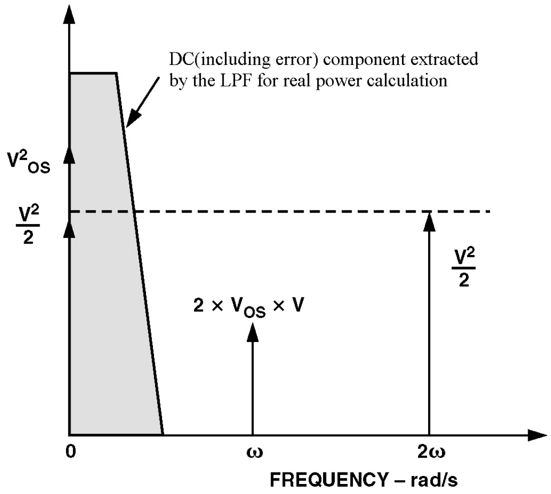

Figure 11. Effect of Input Offset on RMS Calculation

Offset calibration is also used to compensate the intrinsic noise integration effect of the RMS calculation.

8. EXPERIMENTAL MODEL

An experimental model was built to analyse the dynamic behaviour of the ADE7758 three phase energy metering ASIC. The schematic include an input module for the three phased 3x380/220Vrms configuration, using current Hall transducers that provide a wide bandwidth for the active and reactive energy metering, and a voltagedivider.
The PC is connected with optical couplers on all the SPI output signals (from the ASIC to the microcontroller or computer): DOUT, VARCFOUT, APCFOUT, IRQOUT, and input signals (from the microcontroller or computer to the metering ASIC): RESETBIN, CSBIN, DIN, SCLKIN. The APCF logic output gives active power information, and the VARCF logic output provides instantaneous reactive or apparent power information.

Figure 12. Experimental Model Using ADE7758

A practical implementation of ADE7758 for a three phased PC based power and energy meter is presented in figure 12. Figure 13 shows a detailed view of the internal structure of the meter. Hardware calibrations were made in order to obtain adequate measured values using the evaluation software provided by the ASIC manufacturer.

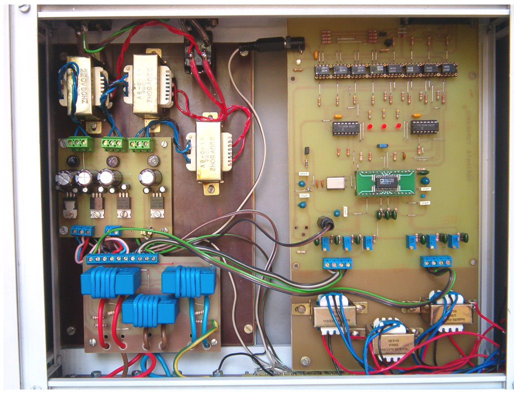

Figure 13. Experimental Model - Detailed View

CONCLUSIONS

ADI energy metering ASICs represent a challenging choice in the energy metering, gathering together high precision performances, reliability, new technology and acceptable price. The conclusion of this study is that ADI ASICs for energy metering are the best choice for specific design. This study was made using an original design for a digital power and energy meter based on ADE7758 from Analog Devices Inc.

REFERENCES

Analog Devices, Inc. - Energy Measurement IC and System Solutions, Last Updated: 08/2005; http://www.analog.com/Analog_Root/static/pdf/dataConverters/SelectionGuides/;

Analog Devices, Inc. - ADSST-EM-1010 (SALEM - 1P) SINGLE-PHASE ELECTRONIC ENERGY METER product brief, January 2001;

Analog Devices, Inc. - ADSST-EM-2010 (SALEM - 3PL) Low Cost Three Phase Energy Meter, http://www.analog.com/UploadedFiles/Product_Briefs;

Analog Devices, Inc. - Evaluation Board Documentation ADE7758 Energy Metring IC, Preliminary Technical Data EVAL-7758EB, august 2003;

Analog Devices Inc. - Poli Phase Multifunction Energy Metering IC with per Phase Information, ADE 7758, september 2004, http://www.analog.com;

Moulin E - RMS Calculation for Energy Meter Applications Using the ADE7756 Application Note (AN-578), february 2003, http:/www.analog.com;