DC-DC STEP-UP/DOWN CONVERTER USED TO DESIGN A SWITCHING POWER SUPPLY
PART B: Design Example, PSpice Simulation, Experimental Results, Practical Considerations and Conclusions

Adriana FLORESCU, Constantin RADOI
"Politehnica" University of Bucharest
Faculty of Electronics, Telecommunications and Information Technology
Bd. Iuliu Maniu 1-3, Bucharest, Romania
adriana.florescu@home.ro, cradoi@elia.pub.ro

Abstract – The paper presents a DC-DC step-up/down converter used in switching power supply with monolithic switching regulator control circuits. The paper completely describes the design of the switching power supply starting with the simplified mathematical theory of the DC-DC step-up/down converter, getting on with the general description of MC34063 and μA78S40 operation modes and then with the mathematical theory of the DC-DC step-up/down converter in boundary conduction mode controlled by the switching regulation control circuits, the PSpice simulation of the whole switching power supply, a numerical example and ending with it's practical implementation. Conclusions about the efficiency of the switching power supply are drawn and some practical considerations are also included.

6. DESIGN EXAMPLE OF SWITCHING POWER SUPPLY WITH STEP-UP/DOWN CONVERTER

The design data are: V_{in} = 7,5V…14,5V, V_{out}=10V, I_{out} = 120 mA, f_{min}= 50 kHz, $V_{ripple(p-p)}$ = 1%V_{out}=100mV_{p-p}. A DC-DC step-up/down converter is necessary and MC 34063 switching regulation control circuit is enough for this application.
The steps of the algorithm for this design example are:

1. The ratio of switches Q_1 and Q_2 conduction t_{on} versus biases diodes D_1 and D_2 conduction t_{off} is determined using equation (7):

$$\frac{t_{on}}{t_{off}} = \frac{V_{out}+V_{F(D1)}+V_{(FD2)}}{V_{in(min)}-V_{sat(Q1)}-V_{sat(Q2)}} = \frac{10V+0{,}6V+0{,}6V}{7{,}5V-0{,}8V-0{,}8V} = 1{,}9 \qquad (17)$$

2. The total switching cycle time of Q_1 and Q_2 is:

$$T_{(max)} = t_{on(max)} + t_{off} = \frac{1}{f_{min}} = \frac{1}{50kHz} = 20\mu s \quad (18)$$

3. From equations (17) and (18), on-time t_{on} and off-time t_{off} of the output switching transistors Q_1 and Q_2 are obtained:

$$t_{off} = \frac{T_{max}}{\frac{t_{on}}{t_{off}}+1} = \frac{20\mu s}{1{,}9+1} = 6{,}9\mu s \qquad (19)$$

$$t_{on} = T_{max} - t_{off} = 20\mu s - 6{,}9\mu s = 13{,}1\mu s \qquad (20)$$

Switching transistors Q_1 and Q_2 minimum duty ratio value $D=t_{on}/T$ is:

$$\frac{t_{on}}{T_{(max)}} = \frac{13{,}1\mu s}{20\mu s} = 0{,}655 < \frac{6}{7} = 0{,}857\,. \qquad (21)$$

Note that the minimum duty ratio value in equation (21) above respects MC34063 data catalogue sheets [5] and doesn't exceed the maximum 6/7 ratio that represents the charge-to-charge and discharge timing of external timing capacitor C_T.

4. The external timing capacitor C_T equation is given in MC34063 data catalogue sheets [5]:

$$C_T = \frac{I_{chg(min)}}{V_{rippleCT}} \cdot t_{on} = \frac{20 \cdot 10^{-6} A}{0{,}5V} \cdot 13{,}1\mu s = 524pF \quad (22)$$

Use a standard C_T=510pF capacitor.

5. The peak switch current is calculated with equation (9):

$$I_{pk(switch)} = 2 I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right) = 2 \cdot 120mA \cdot (1{,}9 + 1) = 0{,}696A \quad (23)$$

6. Since the maximum on-time and peak switch current are known from equations (20) and (23), the minimum value of inductance L can now be calculated with equation (11):

$$L_{min} = \frac{V_{in(min)} - V_{sat(Q1)} - V_{sat(Q2)}}{I_{pk(switch)}} \cdot t_{on} =$$

$$= \frac{7{,}5V - 0{,}8V - 0{,}8V}{0{,}696\ A} \cdot 13{,}1\mu s = 111\ \mu H$$

(24)

An inductance L= 120 µH >L_{min} was selected to obtain the correct continuous conduction operation mode of the DC-DC step-up/down converter.

7. From previous equation (24), a value for the current limit resistor R_{sc} can be determined by using the current limit level of $I_{pk(switch)}$ when V_{in}=12V:

$$I'_{pk(switch)} = \frac{V_{in} - V_{sat(Q1)} - V_{sat(Q2)}}{L_{min}} t_{on(max)} = \quad , \quad (25)$$

$$= \frac{14{,}5V - 0{,}8V - 0{,}8V}{120\mu H} \cdot 13{,}1\mu s = 1{,}41A$$

then the limit resistor value is given by the next equation from MC34063 data catalogue sheets [5]:

$$R_{sc} = \frac{0{,}33}{I'_{pk(switch)}} = \frac{0{,}33}{1{,}41} = 0{,}23\Omega \quad (26)$$

Use a standard R_{sc}= 0,24 Ω

8. A minimum value for an ideal output filter capacitor is given by simplified equation (16):

$$C_0 = \frac{I_{out}}{V_{ripple(p-p)}} t_{on} = \frac{120mA}{100mV_{p-p}} \cdot 13{,}1\mu s = 15{,}7\mu F$$

Ideally this value of C_0 would satisfy the design goal, however, a solid tantalum capacitor of this value will have a typical ESR of 0.3 Ω which will contribute an additional 209mV of ripple. Also there is a ripple component due to the gain of the comparator equal to :

$$V_{ripple(p-p)} = \frac{V_{out}}{V_{ref}} \cdot 1{,}5 \cdot 10^{-3} = \frac{10V}{1{,}25V} \cdot 1{,}5 \cdot 10^{-3} = 12mV$$

The ripple components are not in phase, but can be assumed to be for a conservative design. It becomes apparent that ESR is the dominant factor in the selection of an output filter capacitor. Usualy, an additional LC filter is indicated to diminish $V_{ripple(p-p)}$ until design input data are obtained.

A tantalum capacitor C_0= 330µF with an ESR=0,12 Ω was selected to satisfy this design example by the following:

$$ESR = \frac{V_{ripple(p-p)} - (I_{out}/C_0) \cdot t_{on} - (V_{out}/V_{ref}) \cdot 1.5 \cdot 10^{-3} V}{I_{pk(switch)}}$$

9. The nominal output voltage V_{out} =5V is programmed by R_1 and R_2 resistor divider in order to obtain the comparator output error voltage error u_C=V_{ref} – kV_{out} = 0, where $k = R_1/(R_1 + R_2)$. It results:

$$V_{out} = V_{ref}/K = V_{ref}[(R_2/R_1) + 1] = 1{,}25V \cdot [(R_2/R_1) + 1]$$

(27)

The MC34063 data catalogue sheets indicates that the current through resistor R_1 must be lower than 900µA in order to protect the switching power supply. It results $R_1 = 1{,}25V / 900\mu A = 1{,}38k\Omega$ and a standard value R_1=1,3k Ω is chosen.

From equation (27) and knowing the value of resistor R_1,

the value of resistor R_2 is:

$$R_2 = R_1[(V_{out}/1{,}25V) - 1] = 1{,}3k\Omega \cdot [(10V/1{,}25V) - 1] = 9{,}1k\Omega$$

,(28)

which is a standard value.

10. Transistor Q_1 is driven into saturation with an amplification factor β_F=20 at an input voltage of 7.5V. The required base current is:

$$I_B = \frac{I_{pk(switch)}}{\beta_F} = \frac{0{,}696A}{20} = 35mA$$

The value for the base-emitter turn-off resistor R_{BE} is determined by:

$$R_{BE} = \frac{10\beta_F}{I_{pk(switch)}} = \frac{10 \cdot 20}{0{,}696A} = 287\Omega$$

Standard R_{BE} =330 Ω resistor was selected. Additional base current required due to R_{BE} is:

$$I_{R_{BE}} = \frac{V_{BE(Q1)}}{R_{BE}} = \frac{0{,}8V}{300\Omega} = 3mA$$

$$R_B = \frac{V_{in(min)} - V_{sat(driver)} - V_{R_{SC}} - V_{BE(Q1)}}{I_B + I_{R_{BE}}} =$$

$$= \frac{7{,}5V - 0{,}8V - 0{,}15V - 0{,}8V}{(35+3) \cdot 10^{-3} A} = 151\Omega$$

A standard R_B=150 Ω was used.

The basic schematics that results after the design above which correspond to the basic configuration of DC-DC step-up/down converter in fig.1 is presented in fig.4.

7. PSPICE SIMULATION OF DESIGNED SWITCHING POWER SUPPLY

PSpice under ORCAD was used to software verify the designed switching power supply with MC34063 that controles the DC-DC step-up/down converter. Subcircuit for MC34063 was included. PSpice circuit model is given in fig.5. The most important simulation result is output voltage Vout waveform in fig.6 that proves the stability of the switching power supply. The average value of Vout is of 10.5V obatined after 2.5ms of transient response. The output voltage ripple Vripple(p-p) is arround 0.8V, eight times bigger than the given design value $V_{ripple(p-p)}$ = $1\%V_{out}=100mV_{p-p}$. This bigger value can be explained observing that fig.4 doesn't include the optional suplementary LC filter strongly indicated in MC34063 data catalogue sheets because of limitation in designing the internal comparator and because of suplimentary output voltage ripple introduced by the output capacitor filter.

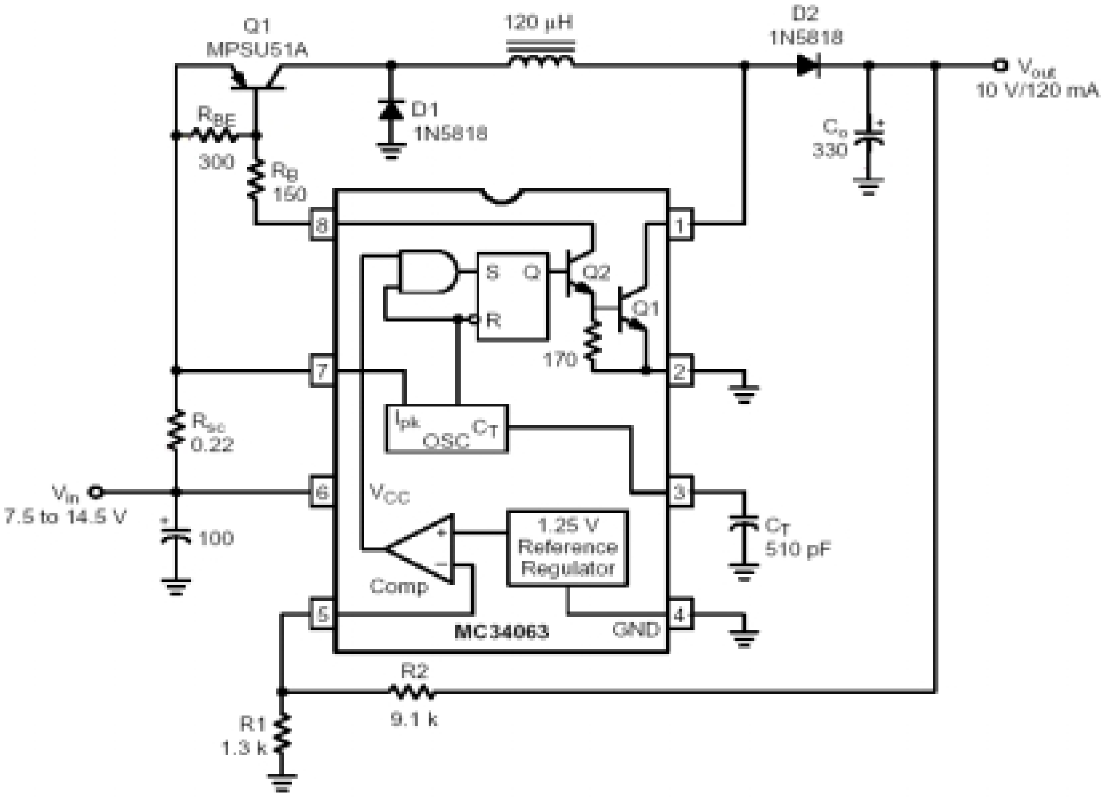

Fig.4. Basic schematics of switching power supply

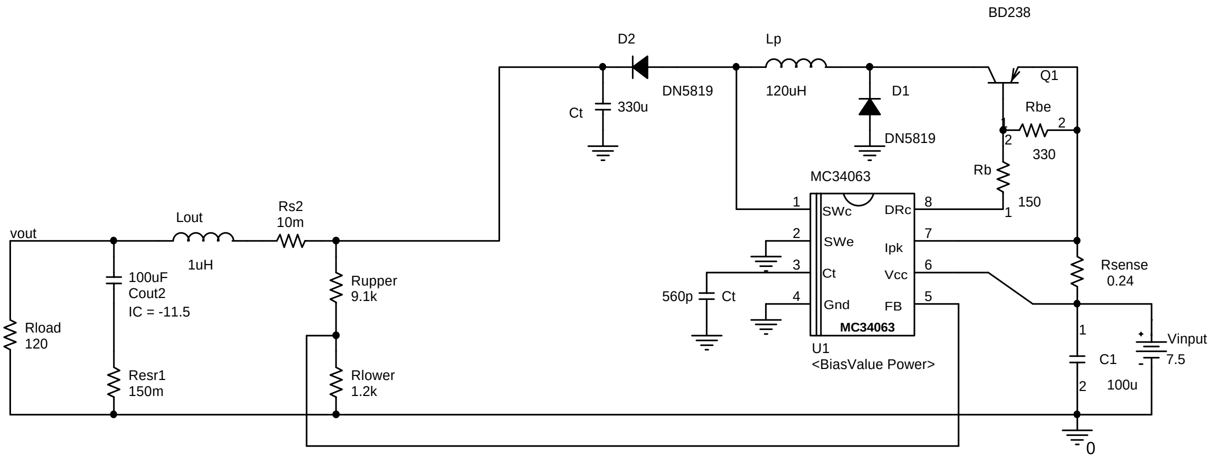

Fig.5. PSpice circuit model for the designed switching power supply

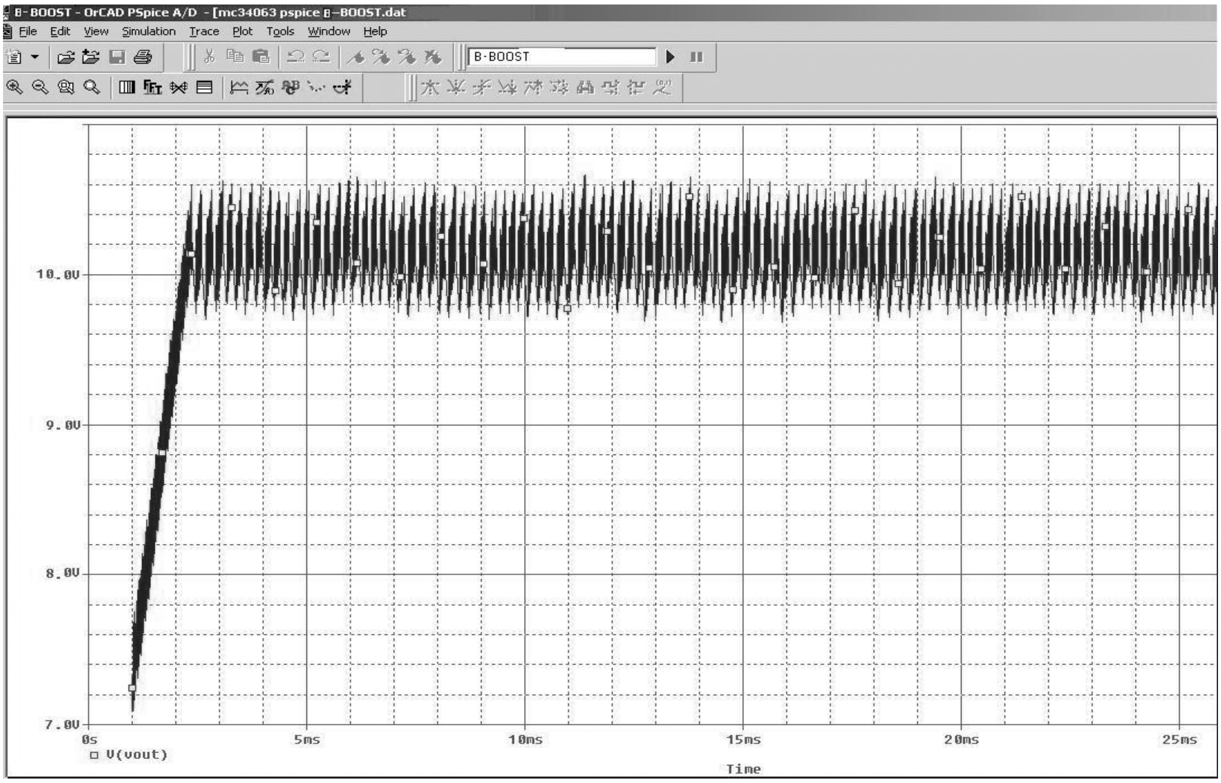

Fig.6. Output voltage V_{out} obtained with PSpice simulation

8. EXPERIMENTAL RESULTS

The final schematics for the designed switching power supply with MC34063 switching regulator control circuit for DC-DC step-up/down converter was obtained adding to fig.4 shortcircuit protection resistors of 5.6KΩ and small value resistors of 1Ω for an easy measurement of voltages in different points of the schematics. Input voltage V_{in}=6.5V and output voltage V_{out} arround 10V waveforms on digital two-channels oscilloscope PSC64i are in fig.7.

These waveforms are the most relevant for a switching power supply. Note that V_{in} is lower than the minimum 7.5V initial design data the circuit still keeps it's nominal output voltage design data V_{out}=10V. The same operation stability was practicly observed on the oscilloscope for an input voltage V_{in}=16V, higher than the maximum 14.5V initial design data. Output power is of 1.2W.

Other relevant waveforms that can be teoreticaly confirmed are shown in fig.8, 9 and 10.

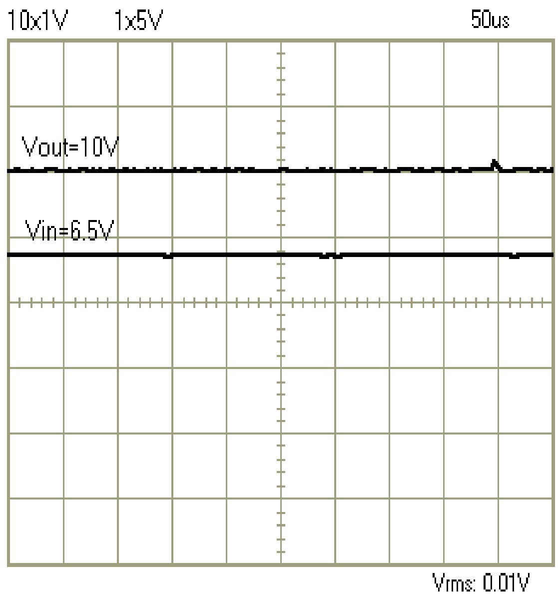

Fig.7. Input voltage V_{in} and output voltage V_{out}

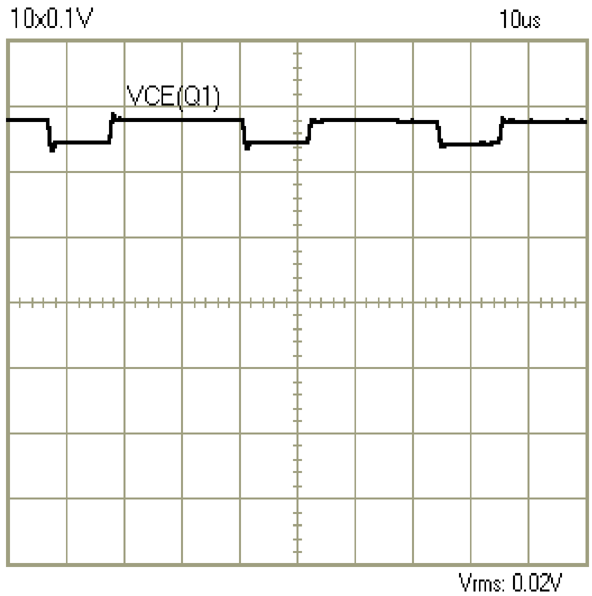

Fig.8. Voltage V_{CE} across switch Q_1

waveforms

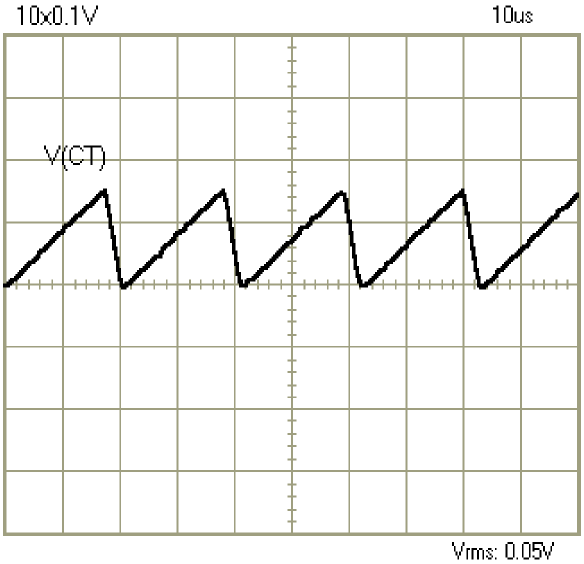

Fig.9. Voltage V_{CT} across external timing capacitor C_T

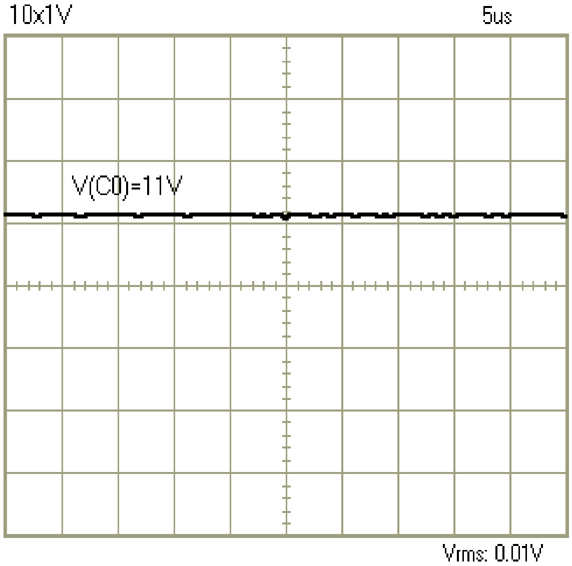

Fig.10. Voltage V_{C0} across output filter capacitor C_T

9. PRACTICAL CONSIDERATIONS

The design equations for L_{min} were based upon the assumption that the switching regulator is operating with a fixed input voltage, maximum output load current and a minimum charge-current oscillator. Typically the oscillator charge-current will be greater that the specific minimum of 20μA, thus t_{on} will be somewhat shorter and the actual LC operating frequency will be greater than predicted f_{min}. The voltage drop developed across the current-limit resistor R_{sc} was not accounted for in the ratio t_{on}/t_{off} and L_{min} formulas. This voltage drop must be considered when designing high current converters

that operate with an input voltage of less than 5V. High frequency circuit layout techniques are imperative with switching regulators. To minimize EMI, all high current loops should be kept as short as possible using heavy copper runs. The low current signal and high current switch and output grounds should return on separate paths back to the input filter capacitor. The R_1 and R_2 output voltage divider should be located as close to the integrated circuit as possible to eliminate any noise pick-up into the feedback loop. The circuit diagrams were purposely drawn in a manner to depick this. All circuits used permalloy power toroid cores for the magnetics where only the inductance value is given.

10. CONCLUSIONS

The goal of this paper was to obtain simple and complete switching power supplies with MC34063 or μA78S40 monolithic switching regulator subsystems used to control DC-DC step-up/down converter.
The paper was split in Part A and Part B. Part A included a brief introduction, basic operation and simplified mathematical theory of DC-DC step-up/down converter, general and functional description of monolithic switching regulator control circuits MC34063 and μA78S40 and mathematical theory of DC-DC step-up/down converter controlled by them. Part B included a design example of switching power supply with step-up/down converter, the PSpice simulation of designed switching power supply, some relevant experimental results, some practical considerations and the final conclusion which is that mathematical theory fits with the simulation and experimental results.
The circuit performance data shows excellent line and load regulation. There is some loss in conversion efficiency over the basic step-down or step-up circuits [1], [2], [3], [4] due to the added switch transistor and diode "on" losses. However, this unique converter demonstrates that with a simple inductor, a step-up/down converter with current limiting can be constructed.

REFERENCES

[1]. Florescu A., Radoi C., *DC-DC Converter with Modern Monolithic Control Circuits,* Proceedings of 7th International Conference on Applied and Theoretical Electricity ICATE 2004, ISBN 973-8043-554-4, October 14-15, 2004, Baile Herculane, Romania, pp. 214-223

[2]. Florescu A., *Switching Power Supply with Monolithic Switching Regulator Subsystems and DC-DC Step-Up Converter,* Proceedings of 4th International Symposium „ Advanced Topics in

Electrical Engineering" (ATEE 2004), ISBN 973-7728-31-9, November 25-26, 2004, Bucuresti, Romania, pp.249-262

[3]. Florescu A., Radoi C., *Surse in comutatie realizate cu convertor c.c.-c.c. cu raport de transformare oarecare,* Proceedings of SNET'05, May 12-15, 2005, Bucuresti, Romania

[4]. Radoi C., Drogoreanu V., Grigore V., Florescu A., s.a., *Electronica si Informatica Industriala. Aplicatii practice*, Editura Tehnica, Bucuresti, 1997

[5]. ***ON Semiconductor Components Catalogue, April 2002