COMPACT MODELING OF PASSIVE ON CHIP COMPONENTS - EUROPEAN RESEARCH PROJECT FP5/IST/CODESTAR

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Abstract— *The paper presents the main scientific objectives and the achievements of the FP5/IST European research project entitled "CODESTAR - Compact modeling of on-chip passive structures at high frequencies". The project goal was the development of a better Electronic Design Automation - EDA tool dedicated to the signal integrity design verification of passive on-chip structures, including interconnects on RFICs. Design, fabrication, and characterization of dedicated test structures was carried out, in order to validate the CODESTAR-code. The matching between experimental and simulation results had proven the project success.*

Keywords: *compact models, EDA, RFIC, interconnects, passives, signal integrity verification, test structures.*

1. INTRODUCTION

With the further downscaling of the IC technology, the operational frequencies of the signals are in the GHz range. As a consequence, the use of lumped-element parameters for the simulation of IC designs is too crude to generate reliable lay-outs. The lumped element models with parameters obtained by static field computation ignore many effects that become pronounced at high frequencies. In other words: interconnects and integrated passives behave qualitatively different at high frequencies as they do at low frequencies.

The fact that high frequency issues can no longer be ignored in IC design has urged the contributors to the International Technology Roadmap for Semiconductors (ITRS, http://*www.itrs.org)* to declare the high-frequency modeling (> 5 GHz) as a *grand challenge.* It should be solved in order to continue the pace of progress that was witnessed in the last three decades.

To accelerate the design of on-chip structures and interconnects the development of new modeling algorithms is needed. This task was addressed by a European joint research project entitled *CODESTAR (http://www.imec.be/codestar)* and carried out within Fifth Framework Program, the thematic component Information Society Technologies (IST). Following three principles drove the project:

· In order to capture the high-frequency effects, full wave electromagnetic field is considered. In particular, this means that no restrictive assumptions are implemented a priori.

· Experimental data provides hardware validation of the developed modeling methodology.

· Computation times should be in an acceptable range. Considering the complexity of the problem this will lead to a trade-off between speed, accuracy and predictability.

2. OBJECTIVES OF THE PROJECT

The main goal of the CODESTAR project is the development of a code dedicated to automatic extraction of compact electric models for passive on-chip structures. The code is a path from layout (cif or GDSII file) to circuit (SPICE format).

First, a detailed electromagnetic analysis of each passive structure is carried out. The outcome of the field solver is a full net list or a semi-state detailed description of the structure. Usual, the size of the model is too large to be useful and therefore a systematic order reduction must be done. The resulting compact model is inserted back into the full design scheme and the design cycle can be pursued.

The project is sub-divided in five major building blocks (work-packages), as indicated in figure 1. Two of them, i.e. the "Maxwell solver" and "Reduced order modeling" have a strong interdisciplinary research character.

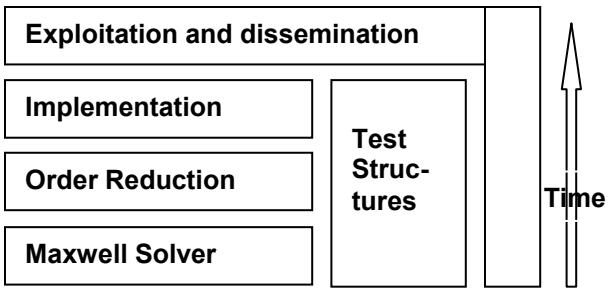

Fig.1. Codestar Work Packages

"Implementation" aims the software development itself, while "Test structures" deals with the input from industrial users and code benchmarking. Finally, "Exploitation and dissemination" aims to use in a commercial and non-commercial manner the research results.

3. FIELD SOLVERS

The following solvers have been selected for an in-depth study and for being applied to on-chip integrated passives and interconnect: **The Lattice-Gauge Solver (LG)** by MAGWEL**; The Finite-Integrals Technique Solver (FIT)** by LMN; **The Finite-Difference Time Domain Solver (FDTD)** by RUG; and **The Partial-Equivalent Electric Circuit Solver (PEEC)** by TU/e [1].

The LG solver uses as fundamental degrees of freedom, the electromagnetic scalar potential and the vector potential. The gauge condition is respected in the Coulomb gauge and ghost field degrees of freedom were added in order to create a well-defined mathematical problem. The solver core has numerous external libraries implemented and tested. A very successful linear kernel was obtained by combining the NAG linear solver library that allows the permutation and row/column ordering algorithms of Duff and Koster - Harwell Subroutine Library- Hyprotech [2].

The Finite-Integration Technique uses the electric and magnetic fluxes and line integrals on grid elements (faces and branches of Yee type cell-grids) as basic degrees of freedom. The approach is well established for the simulation of insulators and conductors, while semiconductors are emulated as moderately conducting materials. An original and efficient numerical method called "dual Finite Integration Technique" (dFIT) was developed as an improved version of FIT. As in FIT, in the new approach, the global variables are used as DOFs, but unlike the FIT, the Hodge operator is obtained by Galerkin projection, using shape functions, as in the Withney (Edge) Finite Element Method. Using both staggered grids as graphs for the electric network and for the magnetic network as well, the new method allows an efficient accuracy control. The dual (complementary) approach allows the effective control of an adaptive procedure for global and local mesh refinement. dFIT accelerates the solution process, preliminary tests showing that there are 50 times less DOFs needed to obtain the same solution accuracy as in FIT [3].

4. ORDER REDUCTION

To solve real complex problems, an original methodological approach called *ALROM (All Level Reduced Order Modeling)* has been developed by PUB-LMN. The ALLROM strategy consists of four stages: *macro-modeling, a-priori ROM*, *on the fly ROM* and *a-posteriory ROM.*

The *macro-modeling phase* is the first step of model building and it requires decisions related to the computational domain clipping, geometric and material idealizations, and phenomenon idealization.

The *a-priori ROM* stage consists mainly in applying a numerical method to discretize the phenomenological model (having an infinite number of dofs) built in the macro-modeling stage. Thus, the number of dofs becomes a finite one. One of the new implemented innovative aspects is related to the boundary conditions. Up to now, most high frequency models are based on scattering S parameters, not suitable for the coupling with extern lumped (SPICE) circuits. The innovative aspect consists of using the "electromagnetic circuit element" concept, which ensures a natural field-circuit coupling [4].

The next stage is the *reduction on the fly*. This reduction is related to the solving of the system of equations assembled previously. The solving may be carried out either in the time domain, or in the frequency domain. To obtain a competitive code, numerical procedures of acceleration and preconditioning have been used. The solution obtained after this step can be used to check the quality of the discretization, and to refine it in order to obtain a more accurate solution [5].

The *a-posteriori reduction* uses classical explicit, or implicit like Krylov type ROM methods. Another possibility is to use the truncated balanced reduction method (TBR) which starts from the modal analysis. Last, but not least, the frequency domain response can be used as input for an interpolation/fitting procedure, which is able to find an approximation of the transfer matrix. All these methods can be chained in order to obtain a smaller and smaller model. To find the best ROM method, a dedicated software package ROM-Work-Bench was developed [1].

5. TEST STRUCTURES

The specifications of the test structures were defined in agreement with the end-users, the developers and the characterization engineers. Besides the processing of CMOS (> 100 nm) and BICMOS structures, measurements will be performed on (sub-) 100 nm CMOS devices with integrated back-end passives (RF-CMOS). The structures were characterized using state-of-the-art on-wafer S-parameter measurement techniques. Finally, benchmark simulations were run to evaluate the capabilities and limitations of both commercially available tools and the newly developed tool. IMEC and Austriamicrosystems has provided benchmark reference data for series of test cases. Two main groups of test cases have been proposed:

1. **Standard Structures:**
   a. Meander resistors (***RPOLY2***), Metal-Oxid-Metal Capacitors (***CMIM***), and Spiral Inductors (SP-SM).
   b. Transmission line structures (***U-COPL***) in Al/Oxide, Al/Lowk, Cu/Oxide and Cu/Lowk, to cover high frequency applications of advanced interconnects.
2. **Challanging Structures** comprise more complex structures, such as
   *a. LL Cells (**SP-CPL**):* The coupling between two identical inductors separated by different distances is examined by these structures
   *b. LC Cells (**SP-C**):* The resulting impedance of a capacitor connected in series with a spiral inductor is examined by these structures
   c. Substrate coupling analyses structures: The signal at a receptor electrode arrived through the substrate from an injector electrode is examined by these structures.
   d. RF – Pads: RF pads provide a low reactance interface point for connecting the internal circuitry through the bond wire and package leads to the application environment.

Full characterization of the standard structures such as resistors, capacitors and inductors have been done, including intensive analysis of the correct de-embedding strategy.

6. PROJECT ACHEIVEMENTS

The main CODESTAR achievement is the development of the computer program dedicated to compact models extraction. This code implements the techniques of ALROM strategies, setting-up a bridge from cif or GDSII to SPICE, and it has following **committed** /*actual* features:

- **Read** geometry (*layout.cif*) and physical (*technology.sipp*) files;
- The developed code was tested on several benchmark structures including **spiral inductors and interconnects** actually *meander resistors, capacitors, inductors transmission lines and challenging structures*;
- **Large mesh (> 64 000 nodes),** actually, initial virtual meshes *having > 1 million nodes* were used;
- **Imposed accuracy (<5%),** actually *<5% at the standard structures, and <20% in the challenging structures* (less than measurement + technology errors);
- Large **frequency range: 0 - 10/20 GHz,** actually *0 - 30/40 GHz***;**
- Reasonable simulation time: **< 3 hours**, actually *< 1 hour in the most cases, <160 min. in the challenging cases***;**
- Order **reduction from >100 000 to <30 000**, *actually <11 DOFs after final ROM step***;**
- **Write** equivalent ***SPICE net-list*** of reduced order model;
- **Matching** between ***measurement and (SPICE) simulation*** results.

These achievements prove a clear advance of the state-of-the-art in the area of high-frequency compact models for passive on-chip structures.

The Table 1 and Fig. 2 presents numerical results of simulation compared with experimental results for a series of benchmarks.

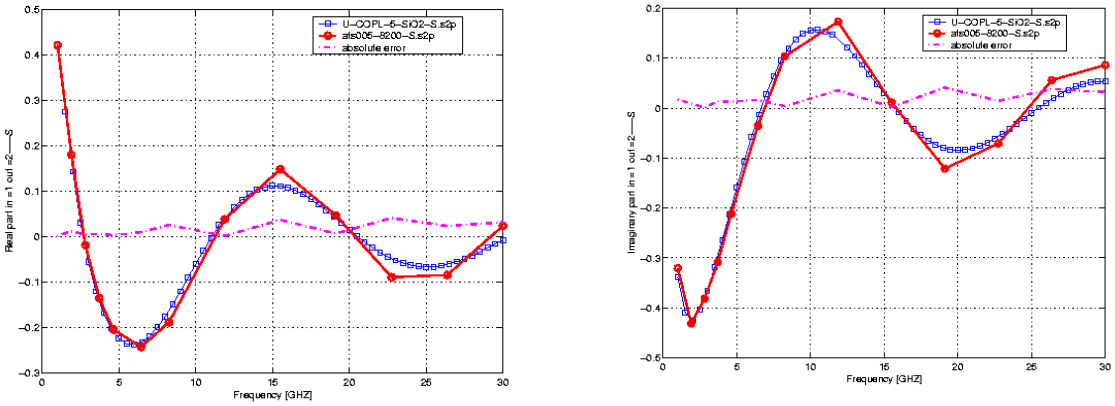

Fig 2. Measured (□) and simulated (●) S parameters versus frequency for the U-COPL benchmark

7. CONCLUSIONS

The new powerful extraction technology was developed with a joint European research effort. A series of innovative techniques allowed us to fulfill the project commitments and state-of-the-art advance. The methodology for compact model extraction proposed by LMN, based on ALLROM approach and the LG solver of MAGWEL were the most efficient solutions, besides those studied within CODESTAR project - actual references. However, extension of field modeling to more complex structures requires the solution of other still open problems, such as automatic domain decomposition, multi-scale, multi-resolution, and parallel solving of large system of linear equations. They will be addressed in next interdisciplinary academic-industry European research projects. You are welcome to join us (see *www.mct.ro/* CEEX).

8. REFERENCES

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Table 1 – Summary of numerical results

Benchmark	***R-POLY2***	***CMIM***	***SP-SM***	***U-COPL AlSiO2***	***SP-CPL***	***SP-C***
Nodes of initial mesh	368,200	833,280	596,068	2,866,441	681,876	458,304
Initial no. of DOFs	2,209,680	4,999,680	3,576,408	17,198,646	4,091,256	2,749,824
Reduced computational domain	48μ × 43μ × 2937 nm	89μ × 89μ × 36μ	330μ × 340μ × 195μ	200μ × 46μ × 17μ	1316μ × 900μ × 507μ	800μ × 800μ × 257μ
Nodes of macro-model	5,940	13,440	9614	7,134	10,998	7392
Macro-model DOFs	19,510	29,925	39920	19,972	43,138	29862
No. of adaptive frequencies (0 -20GHz)	11	15	17	12	15	35
ALLROM CPU time [s]	145	3326	4278	161	2969	9467
Rel. error mes-sim [%]	1.4	2.5	13.6	5.0	15	20
Reduced order (DOFs)	4	4	4	10	4	8
Rel. error red-sim [%]	0.16	0.2	0.5	1.3	0.5	0.5