PWM DC-DC ZERO-VOLTAGE SWITCHING RESONANT BRIDGE CONVERTER

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Abstract: This paper proposes a diagram for a pulsewidth-modulated (PWM) DC-DC bridge converter able to provide a zero-voltage switching (ZVS) for all switches in conditions of load and input voltage large-scale variation. The operating modes, as well as the results of a PSPICE simulation, are also shown and analyzed.

Key-words: bridge converter, PWM, ZVS, DC-DC, zero-current switching (ZCS)

1. INTRODUCTION

This paper proposes a diagram for a PWM DC-DC bridge converter able to provide ZVS for all switches in conditions of load and input voltage large-scale variation. The goals of the paper are: 1) to explain the ZVS bridge converter's diagram; 2) to analyze its operating modes; 3) to draft the design curves and to calculate the optimal design point; 4) to verify converter's performances at various loads and variable input voltages, using PSPICE.
Section 2 shows the functioning principle for this converter. In section 3 we present its analyze performed on continuous duty. The design procedure and an example of optimal model are presented in section 4. Simulation's results are detailed in section 5 and conclusions are given in section 6.

2. OPERATING PRINCIPLE

Figure 1 shows the diagram of a DC-DC bridge converter with isolating transformer. The S_1-S_4 switches are controlled using a complementary fixed frequency (with variable filling factor - PWM). The control signals generate rectangular shaped waves for the V_{AB} between terminals A and B of which negative and positive areas are equal (Figure 2). The proposed control diagram, together with an optimal design, will provide ZVS for the S_2, S_3 şi S_4 switches. Hence, the S1 switch will operate on ZVS from maximal load down to approximately 80% of the load. In order to provide ZVS on S_1 at low loads, an auxiliary circuit is necessary.

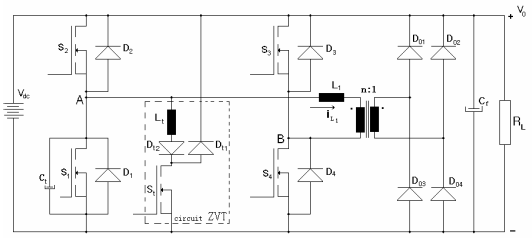

Fig. 1. Diagram of a PWM DC-DC converter

We notice that, in order to provide ZVS at low loads, two circuits of this type are necessary, both of them having transition at zero voltage (ZVT) (Redl, 1994). This circuit's power consumption is very low and it is able to supply zero voltage transition (ZVT) when S_1 is out of ZVS. In this way, the S1 switch will open with ZVT and S_2, not only that will open with ZVS, but also will close with a zero switching current. Figure 2 shows the control signals, the v_{AB} voltage and the I_{L1} current for three different loads. In Figure 2(a) the load is maximal, D = 0,5 and the pulse's width is π. As the load current decreases the pulse's width decreases too, proportionally with a dead zone, which cuts symmetrically the v_{AB} voltage at both ends, with α, as it is shown in Figures 2(b) and 2(c).

2.1. Operating modes

The i_{L1} current, which depends of the load current, operates in continuous conduction mode (TI-CCM) [Figures 2(a) and (b)] as well as in discontinuous conduction mode (TI-DCM) [Figure 2(c)].

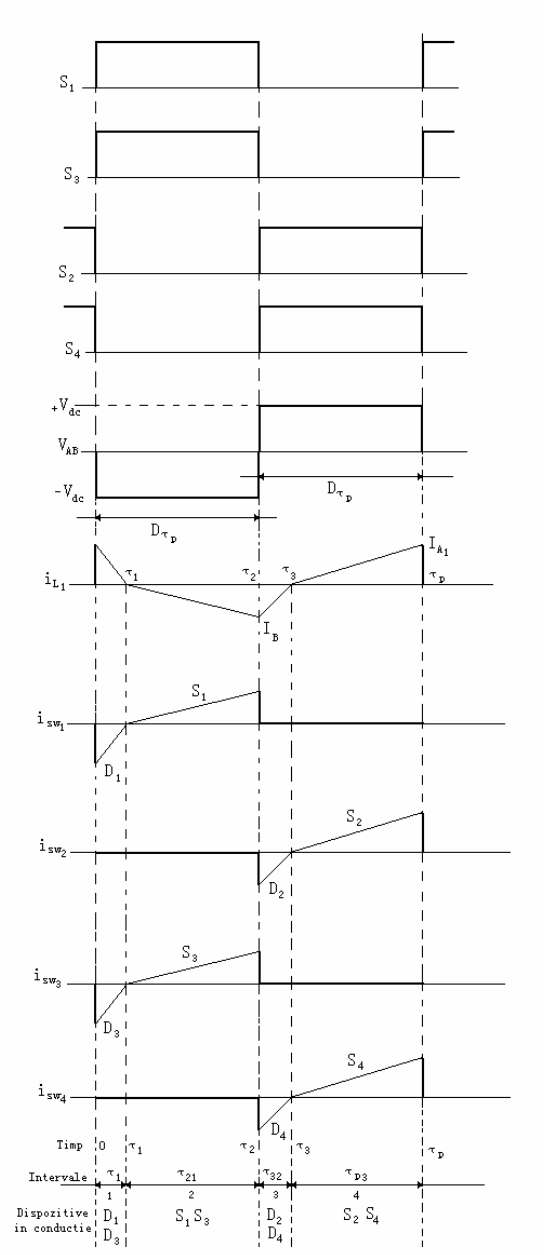

Fig. 2(a). Control signals, voltage and current through L_1 and current on each switch at maximal load (TI-CCM).

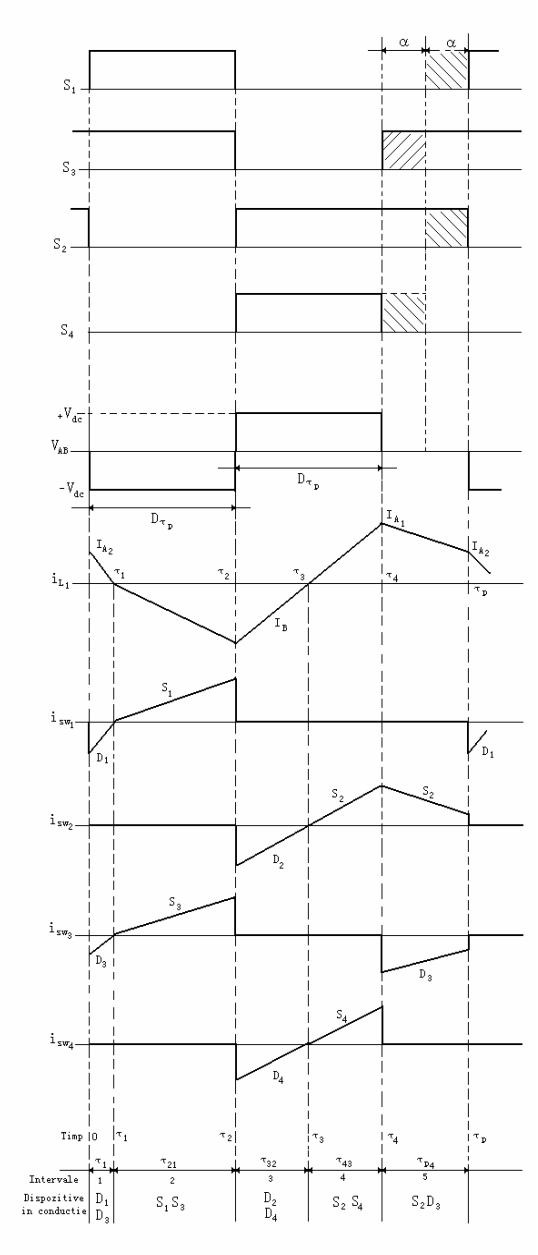

Fig. 2(b). Control signals, voltage and current through L_1 and current on each switch when load is bigger than the transition loads (TI-CCM).

Figure 2(a) shows the wave shapes at maximal load and minimal input voltage. The v_{AB} input voltage is rectangular (D = 0,5). Figures 2(b) and (c) show the wave shapes of v_{AB} voltage, for the current through L_1, for the current on each switch on both operating modes, that is TI-CCM, respectively TI-DCM. For loads smaller than the maximal load and D < 0,5, the control signals on S_1 and S_4 decrease with α. Therefore, each semi-cycle of v_{AB} voltage decreases to $D\tau_p = (\tau_p/2) - \alpha$, where τ_p is the period.

3. THE ANALYSIS

In order to study the converter on both modes (TI-CCM, and TI-DCM), on adopt some simplifying assumptions in order to facilitate the analysis (e.g.: circuit's components are ideal, the DC I/O voltages have insignificant ripple, the rectifier and the output filter are replaced with a rectangular voltage source, etc.). In section 3.1. the general formulas for current via coil L_1 are given.

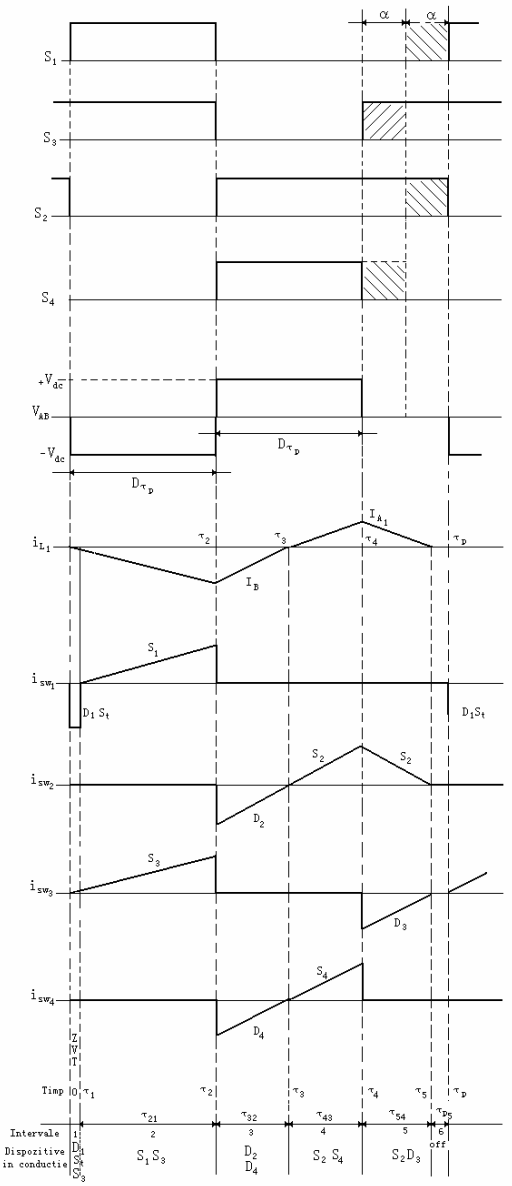

Fig. 2(c). Control signals, voltage and current through L_1 and current on each switch when load is smaller than the transition loads (TI-DCM).

In section 3.2, we obtain the design points and the converter's operational parameters using the formulas for continuous duty.

3.1. General formulas

General formulas for the TI-CCM operational mode [Figure 2(b)]. In this operating mode we have 5 different intervals. The equivalent circuits for these intervals are given in Figure 3.

Interval 1 [Figure 3(a)]: $0 < \tau < \tau_1$, $v_{AB} = -V_{dc}$: the current through L_1 is positive and decreases compared to I_{A2}. Diodes D_1 and D_3 are conducting. The formula for $i_{L1}(\tau)$, under the original assumption $i_{L1}(0) = I_{A2}$, is:

$$i_{L1}(\tau) = I_{A2} - [(V_{dc}+nV_0)/L_1]\tau \quad (1)$$

At the end of this interval $i_{L1}(\tau_1) = 0$.

Interval 2 [Figure 3(b)]: $\tau_1 < \tau < \tau_2$ ($\tau_2 = D\tau_p$), $v_{AB} = -V_{dc}$: switches S_1 and S_3 open with ZVS. The current through L_1 is negative and decreases down to I_B. Formula for $i_{L1}(\tau)$, under the original assumption $i_{L1}(\tau_1) = 0$, is:

$$i_{L1}(\tau) = -[(V_{dc}-nV_0)/L_1](\tau-\tau_1) \quad (2)$$

At the end of this interval $i_{L1}(\tau_2) = I_B$.

Interval 3 [Figure 3(c)]: $\tau_2 < \tau < \tau_3$, $v_{AB} = +V_{dc}$: the current through L_1, which is negative and decreases, goes through the diodes D_2 and D_4. Formula for $i_{L1}(\tau)$, under the original assumption $i_{L1}(\tau_2) = I_B$, is:

$$i_{L1}(\tau) = [(V_{dc}+nV_0)/L_1](\tau-D\tau_p)+I_B \quad (3)$$

At the end of this interval $i_{L1}(\tau_3) = 0$.

Interval 4 [Fig. 3(d)]: $\tau_3 < \tau < \tau_4$ ($\tau_4 = 2D\tau_p$), $v_{AB} = +V_{dc}$: switches S_2 and S_4 open with ZVS. The current through L_1 is positive and increases from 0 up to I_{A1}. Formula for $i_{L1}(\tau)$, under the original assumption $i_{L1}(\tau_3) = 0$, is:

$$i_{L1}(\tau) = [(V_{dc}-nV_0)/L_1](\tau-\tau_3) \quad (4)$$

At the end of this interval $i_{L1}(\tau_4) = I_{A1}$.

Interval 5 [Figure 3(e)]: $\tau_4 < \tau < \tau_p$, $v_{AB} = 0$: switch S_4 closes at τ_4. The current through L_1 decreases from I_{A1} to I_{A2}, its path being via switch S_2 and diode D_3. Formula for $i_{L1}(\tau)$, under the original assumption $i_{L1}(\tau_4) = I_{A1}$, is:

$$i_{L1}(\tau) = I_{A1} - (nV_0/L_1)(\tau-2D\tau_p) \quad (5)$$

At end of cycle S_2 closes and current through i_{L1} will become again $i_{L1}(\tau_p) = I_{A2}$.

The transition from the TI-CCM mode to the TI-DCM mode. Based on the designing point, when the load decreases lesser than the transition load, the iL1 current toggles from the TI-CCM mode [Figure 2(b)] to the TI-DCM mode [Figure 2(c)]. In the transition point we have:

$$\tau_1 = 0,\ I_{A2} = 0,\ i_{L1}(\tau_p) = i_{L1}(0) = 0 \quad (6)$$

General formulas for the TI-DCM operating mode [Figure 2(c)]. Figure 4 shows the two additional equivalent circuits that appear when this operating mode is on.

Interval 1 [Figure 4(a)]: $0 < \tau < \tau_t$: during the very short interval of ZVT, switch S_t opens and a resonant sinusoidal current at semi-cycle passes through D_1 and supplies ZVT for S_1. In order to facilitate the study, the 1st interval, which is very short, is overlooked; we assume that the 2nd interval begins at the moment $\tau = 0$.

Interval 2: $\tau_t < \tau < \tau_2$: vAB = -Vdc and the current through L1 is zero and decreases. The switches S_3 and S_1 (which opened with ZVT) start to conduct.

$$i_{L1}(\tau) = -[(V_{dc}-nV_0)/L_1]\tau \quad (7)$$

Intervals 3, 4 and 5: are identical to those for TI-CCM operating mode; therefore the same equations are available to be used, with an unique exception: at the end of the 5th interval the current through L_1 becomes 0 and S_2 closes with ZCS. We have: $i_{S2} = i_{D3} = i_{L1} = 0$.

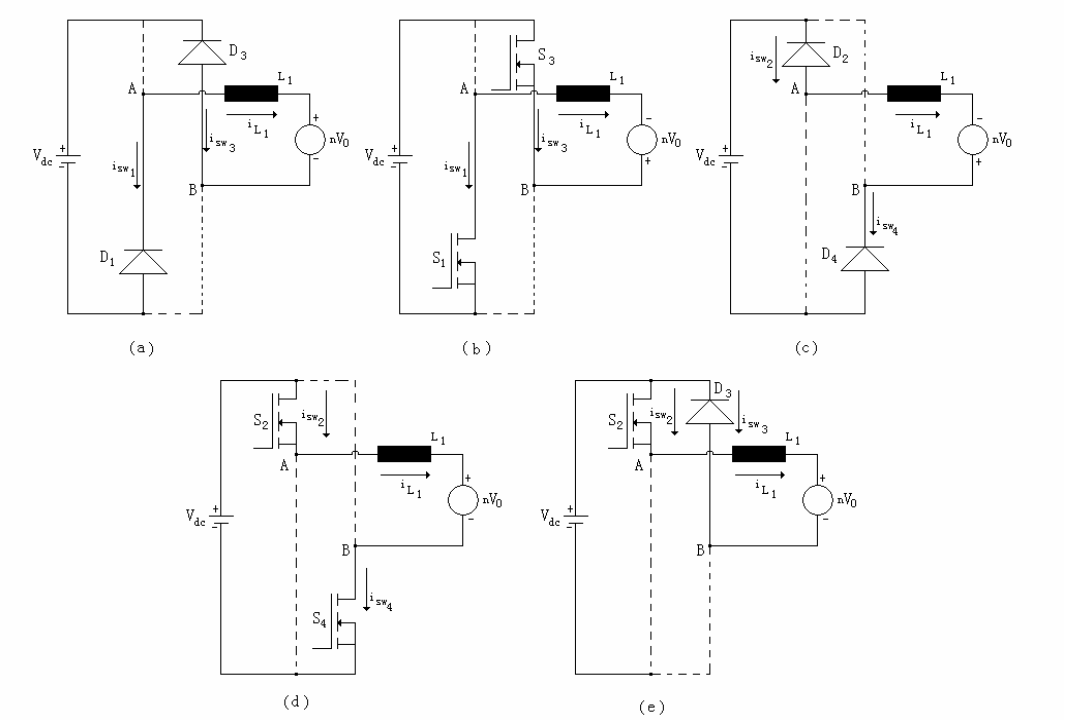

Fig. 3. The equivalent circuits corresponding to TI-CCM mode [Figure 2(b)]. (a) interval 1. (b) interval 2. (c) interval 3. (d) interval 4. (e) interval 5.

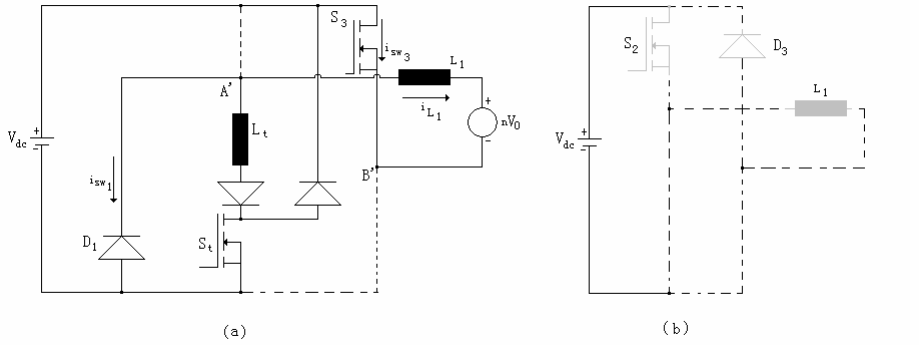

Fig. 4. The equivalent additional circuits corresponding to TI-DCM mode [Figure 2(c)]. (a) interval with ZVT ($0 < \tau < \tau_t$). (b) interval 6.

Interval 6 [Figure 4(b)]: $\tau_5 < \tau < \tau_p$: in this interval the current i_{L1} remains 0 ($i_{L1} = 0$). All the converter's switches and diodes are closed and only the output filter capacitor supplies power on load.

3.2. The Analysis of Continuous Duty

The formulas for continuous duty are derived from the general formulas and the limit conditions. These formulas are divided in two classes: for TI-CCM mode and for TI-DCM mode. All the equations are normalized using the following notations:

$V_b = V_{dc(min)}$ (input minimal voltage)

$P_b = P_{or}$ (output nominal power)

$I_b = P_{or}/V_b$; $t_b = \tau_p$; $L_b = t_b \cdot V_b/I_b$. (8)

The converter's gain is defined as $M = nV_0/V_{dc}$ and it will vary along with the input voltage variation ($M_{max} = nV_0/V_{dc(min)}$). All the values per-unit are denoted with „pu".

The normalized formulas in continuous duty, TI-CCM mode [Figure 2(b)]:

The voltage on coil L1 for each interval is:

interval 1: $L_{1pu}(I_{A2pu}/\tau_{1pu}) = V_{dcpu} + M_{max}$ (9)

interval 2: $L_{1pu}(I_{Bpu}/\tau_{21pu}) = V_{dcpu} - M_{max}$ (10)

interval 3: $L_{1pu}(I_{Bpu}/\tau_{32pu}) = V_{dcpu} + M_{max}$ (11)

interval 4: $L_{1pu}(I_{A1pu}/\tau_{43pu}) = V_{dcpu} - M_{max}$ (12)

interval 5: $L_{1pu}(I_{A1pu}/\tau_{1pu} - I_{A2pu})/\tau_{p4pu} = M_{max}$ (13)

The current balance $i_{L1}(\tau)$ on period τ_1-τ_p is:

$$I_{Bpu}(\tau_{21pu}+\tau_{32pu}) = I_{A1pu}\cdot\tau_{43pu} + I_{A2pu}\cdot\tau_{1pu} + (I_{A1pu}+I_{A2pu})\cdot\tau_{p4pu} \quad (14)$$

The average current on transformer's secondary circuit (at rectifier's output) is: $I_{Bpu}(\tau_{21pu}+\tau_{32pu}) + I_{A1pu}\cdot\tau_{43pu} + I_{A2pu}\cdot\tau_{1pu} + (I_{A1pu}+I_{A2pu})\cdot\tau_{p4pu} = 2P_{opu}/M_{max}$ (15)

The filling factor depends of intervals' time:

$$D = \tau_{1pu}+\tau_{21pu}\,;\ D = \tau_{32pu}+\tau_{43pu}\,;\ (1\text{-}2D) = \tau_{p4pu} \quad (16)$$

The normalized formulas in continuous duty, TI-DCM mode [Figure 2(c)]:

The voltage on coil L1 for each interval is:

$$L_{1pu}(I_{Bpu}/\tau_{21pu}) = V_{dcpu} - M_{max} \quad (17)$$

$$L_{1pu}(I_{Bpu}/\tau_{32pu}) = V_{dcpu} + M_{max} \quad (18)$$

$$L_{1pu}(I_{A1pu}/\tau_{43pu}) = V_{dcpu} - M_{max} \quad (19)$$

$$L_{1pu}(I_{A1pu}/\tau_{1pu}) = M_{max} \quad (20)$$

The current balance $i_{L1}(\tau)$ on period τ_1-τ_p is:

$$I_{Bpu}(\tau_{21pu}+\tau_{32pu}) = I_{A1pu}(\tau_{43pu}+\tau_{54pu}) \quad (21)$$

The average current on transformer's secondary circuit (at rectifier's output) is:

$$I_{Bpu}(\tau_{21pu}+\tau_{32pu}) + I_{A1pu}\cdot(\tau_{43pu}+\tau_{54pu}) = 2\cdot P_{opu}(1-\tau_{p5pu})/M_{max} \quad (22)$$

The filling factor depending of intervals' time is:

$$D = \tau_{21pu}\,;\ D = \tau_{32pu}+\tau_{43pu}\,;\ (1\text{-}2D) = \tau_{54pu}+\tau_{p5pu} \quad (23)$$

4. DESIGN

The continuous duty's formulas are digitally solved using MATHCAD. The design is performed at maximal load, with a minimal input voltage V_{dc} and a filling factor D = 0,5 [Figure 2(a), perfect rectangular wave for v_{AB} and current through L_1 in TI-CCM duty]. The 7 equations of continuous duty (9)-(12) and (14)-(16) have 7 unknown variables (L_{1pu}, I_{A1pu}, I_{Bpu}, τ_{1pu}, τ_{21pu}, τ_{32pu}, τ_{4pu}) and D = 0,5, V_{dcpu} = 1, $I_{A2pu} = I_{A1pu}$ and $\tau_{p4pu} = 0$. The maximal efficiency obtained next to calculations ranges between 0,2 and 0,8, as it is shown in Table 1. It is noticed that for big gains (M_{max}) the current peaks via components are reduced. On the other hand, a big gain involves the increase of risk to loose ZVS on S_4 (which is proportional with τ_{32}) at low loads. In order to provide ZVS for S_4, τ_{32} (the conduction time for D_4) has to be guaranteed as being greater than the minimal value at minimal load. For an optimal design the decrease of maximal current on components and the providing of ZVS for S_4, at minimal load have to be taken into account. In Figure 5 we draw the graph for the coefficient of peak current through L1 when D4 is on conduction ($IA1pu/\tau_{32pu}$), as a function of the gain (M_{max}). The optimization curve's minimal point, M_{max} = 0,5, is selected as designing point able to provide ZVS to S4 at low loads. The filtering capacitor C_f has to be able to reduce the output voltage's ripple at any load. The filter's capacity is calculated at maximal load, for minimal input voltage and a filling factor D = 0,5:

$$C_f = nI_A/(16\cdot f_s\Delta V_0) \quad (24)$$

where n is the transformer's coefficient, I_A is the load current, f_s is the switching frequency and ΔV_0 is the output voltage's ripple.

Table 1. Per-unit design values at maximal load for minimal input voltage (D = 0,5, Vdc = 1pu)

M_{max}	L_{1pu}	I_{A1pu}	I_{Bpu}	τ_{1pu}	τ_{21pu}	τ_{32pu}	τ_{43pu}
0,2	0,024	10	-10	0,2	0,3	0,2	0,3
0,3	0,034	6,66	-6,66	0,175	0,325	0,175	0,325
0,4	0,042	5	-5	0,15	0,35	0,15	0,35
0,5	0,047	4	-4	0,125	0,375	0,125	0,375
0,6	0,048	3,33	-3,33	0,1	0,4	0,1	0,4
0,7	0,045	2,85	-2,85	0,075	0,425	0,075	0,425
0,8	0,036	2,5	-2,5	0,05	0,45	0,05	0,45

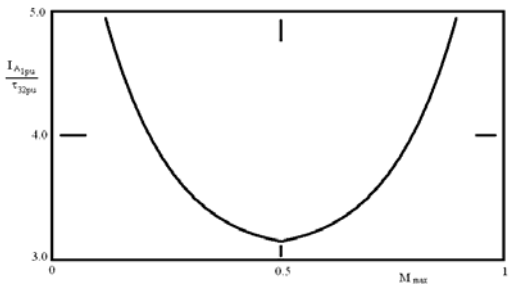

Fig. 5. The optimizing curve for the minimizing of peak current through L_1 as long as the D_4 diode conducts (I_{A1}/τ_{32}).

5. THE PSPICE ANALYSIS

For this study the next values have been taken into account: input voltage V_{dc} = 300–360V, output power P_0 = 500W, load voltage V_0 = 48V, peak-to-peak output voltage's ripple 1% of V_0, switching frequency 10 kHz. Table 2 shows the results of a PSPICE simulation at different loads, and minimal and maximal input voltages. The V_0 output voltage varies as a function of the filling factor D.

Table 2. The results of a PSCPICE simulation for a 500W converter, at various loads, and minimal and maximal input voltages

input voltage	Min V_{dc} = 300V M_{max} = 0,5pu			Max V_{dc} = 360V M_{min} = 0,416pu		
load	100%	50%	10%	100%	50%	10%
D	0,5	0,28	0,13	0,31	0,21	0,10
I_{A1} (A)	6,57	3,85	1,9	4	2,3	1,3
I_{A2} (A)	6,57	0	0	0	0	0
I_B (A)	-6,57	-4,95	-2,2	-5	-3	-1,5
mode	TI-CCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM	TI-DCM

Figure 6 shows the simulation's wave shapes in the two extreme situations, the maximal load at minimal input voltage and 10% load with maximal input voltage. The current's wave shapes through the switching devices demonstrates clearly that these devices opens with ZVS on the whole range of loads (Rashid, 1993).

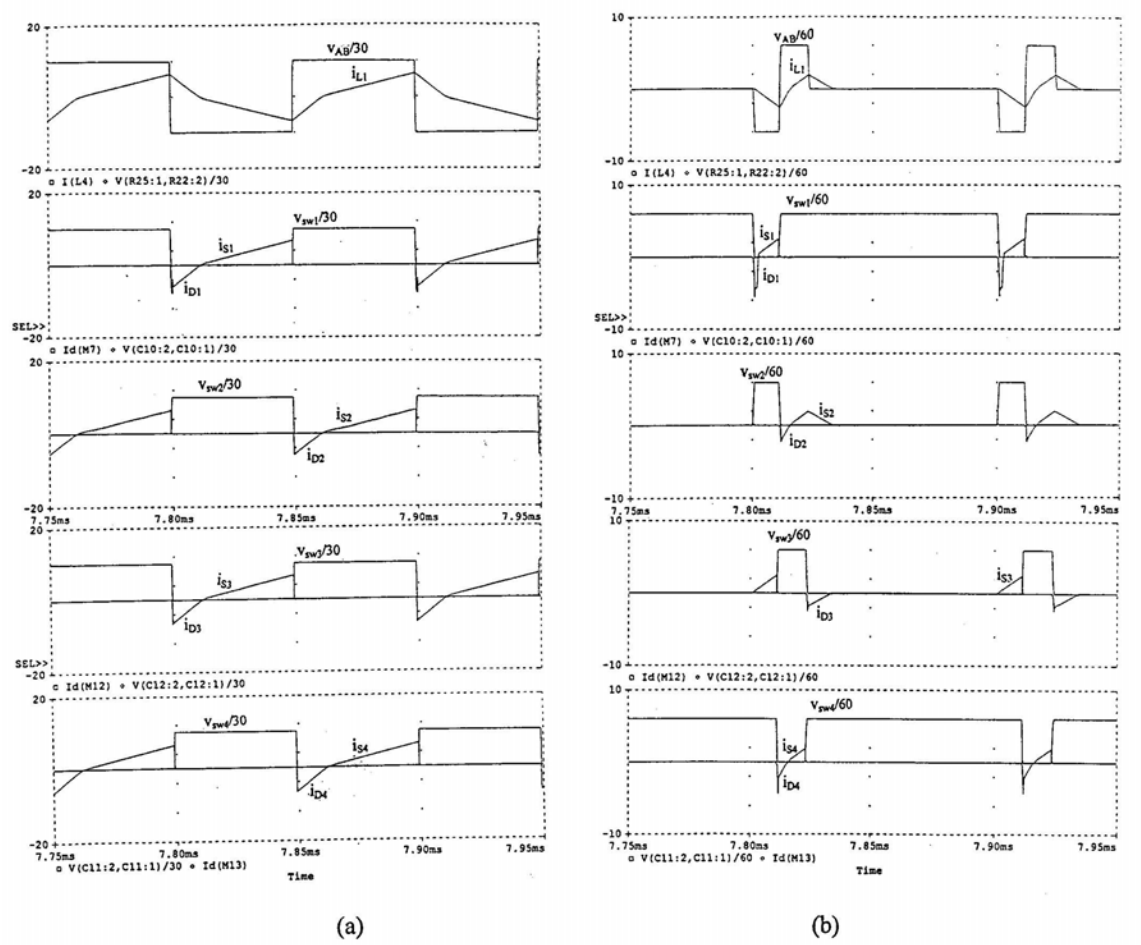

Fig. 6. The results of the PSPICE simulation. v_{AB} voltage, i_{L1} current and switches' wave shapes.
(a) maximal load (500W, $R_L = 4{,}6\Omega$) at minimal input voltage $V_{dc} = 300V$. (b) 10% of load (50W, $V_0 = 48V$, $R_L = 46\Omega$) at maximal input voltage $V_{dc} = 360V$.

6. CONCLUSIONS

This paper proposes a new control diagram, with fixed complementary frequency, for soft switching PWM DC-DC bridge converters. The diagram has been used on a bridge converter equipped with isolating transformer, rectifying bridge and output filtering capacitor. For the designed converter have been presented a detailed analysis as well as a PSPICE simulation. Some of the converter's features are given below:

(1) The control diagram has fixed frequency and variable filling factor;

(2) ZCS is provided on all switches in all the specified conditions and during the load's variation;

(3) Greater efficiencies can be possibly obtained using IGBTs instead of MOSFETs, for the S1-S4 switches. For the output rectifying bridge the use of Schotky diodes is recommended (Diaconescu, 1996; Lucanu 1997), these having a lower voltage drop and a superior switching speed compared to the regular rectifying diodes.

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