THE CMOS GENERIC TRANSLINEAR NETWORK IMPLEMENTATION OF POLINOMIAL APPROXIMATED FUNCTIONS

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Abstract: In this paper are presented several translinear topologies suitable for static and dynamic analog signal processing in mixed-signal chips fabricated in digital CMOS technology and operated at very low supply voltage. The one or two variable objective functions that can be implemented with these translinear topologies, firstly are polynomial approximated and then are decomposed in continued products. Also, the objective functions do not contain time or frequency variables.

Keywords: Analog signal processing circuits, translinear circuits, CMOS analog integrated circuits, low power and low voltage circuits.

1. INTRODUCTION

The existing CMOS technologies provide ample opportunity to integrate entire systems on to a single integrated circuit. To date, the ability to integrate large digital systems has far outweighed the ability to integrate the analog systems. The greatest impediment to analog CMOS VLSI design has been the inability to provide consistent circuit performance over the broad range of requirements for signal gain, frequency response, phase response, delay, power and signal fidelity imposed by analog designs. More, as the power supply voltage for integrated circuits continues to scale down, the analog design in mixed signal environments is becoming more difficult and challenging. Future analog circuits will have to operate successfully at supply voltages slightly higher than the MOS threshold voltage.

So, the suitable topologies for signal processing at such low values of supply voltages are the translinear circuits because are operating in current domain and in this way the very small voltage swings are avoided. The MOS transistors have exponential current-voltage characteristics in weak inversion (or sub-threshold) region. Therefore in these circuits the MOS transistors will operate in this region. The main problems of this operating region are the relatively low speed capability and inferior matching. But these problems are relatively solved in sub-micron technology.

In this paper are presented several CMOS translinear topologies that implement one or two variable objective functions, polynomial approximated and continued products decomposed. one or two variable objective functions. I choose polynomial approximation for objective functions because such function processing leads to implementations with relatively small number of devices, good stability and acceptable errors.

2. MICROPOWER MOS TRANSISTORS IN WEAK INVERSION

In above section was argued that the MOS transistor in low-voltage translinear circuits will operate in weak inversion. It is well known the general expression of drain current of MOS transistor:

$$I_D = \beta \cdot \int_{V_S}^{V_D} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}\, V \quad \text{, with} \tag{1}$$

$$\beta = \mu \cdot C_{ox} \cdot \frac{W}{L} \tag{2}$$

where

W, L	width, length of the channel;
C_{ox}	gate capacitance per unit area;
μ	charge carrier mobility;
Q_i	induced mobile charge in channel;
V_D, V_S	drain, source voltages referred to the local substrate;
V	channel potential.

This expression may be decomposed into:

$$I_D = \beta \cdot \int_{V_S}^{\infty} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}V - \beta \cdot \int_{V_D}^{\infty} \left(-\frac{Q_i}{C_{ox}} \right) \cdot \mathrm{d}V = I_F - I_R \quad (3)$$

where I_F is called forward current (controlled by source voltage V_S) and I_R is called reverse current (controlled by drain voltage V_D).
In weak inversion we have:

$$Q_i / C_{ox} \sim \exp\left(\frac{V_P - V}{V_T} \right) \quad (4)$$

where

V_P	pinchoff voltage which is a nonlinear function of gate voltage V_G and represents the body effect;
V_T	thermal voltage ($k \cdot T / q$).

Thus we have the following proportionality

$$I_F \sim \beta \cdot \exp\left(\frac{V_P - V_S}{V_T} \right)$$
$$I_R \sim \beta \cdot \exp\left(\frac{V_P - V_D}{V_T} \right) \quad (5)$$

and the drain current has the expression

$$I_D = I_S \cdot \exp\left(\frac{V_P}{V_T} \right) \cdot \left[\exp\left(-\frac{V_S}{V_T} \right) - \exp\left(-\frac{V_D}{V_T} \right) \right] \quad (6)$$

or in terms of V_{GS} and V_{GD} as follows

$$I_D = I_S \exp\left(\frac{V_P - V_G}{V_T} \right) \cdot \left[\exp\left(\frac{V_{GS}}{V_T} \right) - \exp\left(\frac{V_{GD}}{V_T} \right) \right] \quad (7)$$

where I_S is specific current (limit of weak inversion). The specific current is proportional to W/L, follows explicitly shown

$$I_S \cdot \exp\left(\frac{V_P - V_G}{V_T} \right) = \frac{W}{L} \cdot I_{\Diamond}(V_G) \quad (8)$$

with $I_{\Diamond}(V_G)$ the zero-bias ($V_{GS} = 0$) current for a square transistor, which represents the body effect.
So, the forward and reverse currents become:

$$I_F = \frac{W}{L} \cdot I_{\Diamond}(V_G) \cdot \exp\left(\frac{V_{GS}}{V_T} \right)$$
$$I_R = \frac{W}{L} \cdot I_{\Diamond}(V_G) \cdot \exp\left(\frac{V_{DS}}{V_T} \right) \quad (9)$$

If $I_R << I_F$, then the MOS transistor is saturated, otherwise the MOS transistor is non-saturated. In figure 1.a are shown the two operation regions for weak inversion, which are defined by the ratios I_D / I_F and V_{DS} / V_T.

Therefore, each of the drain current components (expressed by (9)) of a non-saturated transistor may be relate to an equivalent saturated transistor with gate-source voltage V_{GS} and V_{GD} respectively and the non-saturated transistor may be decomposed into two identical saturated transistors connected anti-parallel. This is symbolically shown in figure 1.b. The transistor that corresponds to reverse current component is shown in dashed line, and represents the effect of the non-saturated operation of the real transistor. This equivalence may be also applied to bipolar transistors, based on the Ebers-Moll model, but it is impractical because of asymmetry of real bipolar transistors.

3. THE CMOS TRANSLINEAR IMPLEMENTATION OF POLYNOMIAL APPROXIMATED OBJECTIVE FUNCTIONS

The objective-functions are first normalised, so that theirs variables to take values only in interval [-1, 1]. Then the one variable normalises functions are approximated by the following methods:

- *MacLaurean* that consist in truncating of MacLaurean series so that the maximum relative error of approximation to be 0.01% ÷ 0.1%. The functions obtained after approximation have the form:

$$f_a(x) = \sum_{i=0}^{N} a_i \cdot x^i \quad (10)$$

with

$$a_k = \frac{1}{k!} \cdot \left(\frac{\partial^k f}{\partial x^k} \bigg|_{x=0} \right) \quad (11)$$

- *Chebyshev* that consist in truncating of Chebyshev series so that the maximum relative error of approximation to be 0.01% ÷ 0.1%. The functions obtained after approximation have form:

$$f_a(x) = \left[\sum_{i=0}^{N-1} c_i \cdot T_i(x) \right] - \frac{1}{2} \cdot c_0 , \quad (12)$$

where the coefficients c_i are given by the formula:

$$c_i = \frac{2}{N} \sum_{k=1}^{N} f\left[\cos\left(\frac{\pi\left(k - \frac{1}{2} \right)}{N} \right) \right] \cos\left(\frac{\pi \mathrm{j}\left(k - \frac{1}{2} \right)}{N} \right) \quad (13)$$

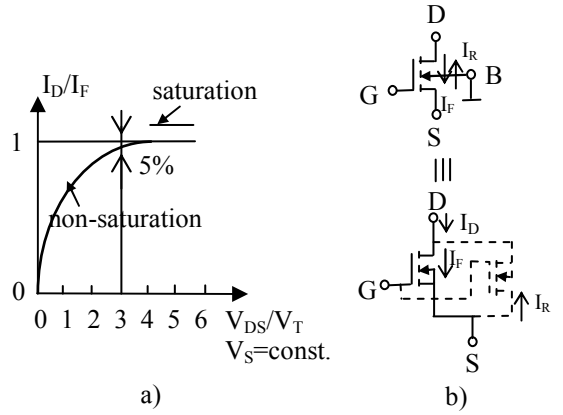

Figure 1. a) The operation regions in weak inversion of the MOS transistor; b) Non-saturated Mos transistor equivalent to two saturated transistors connected anti-parallel.

The $T_i(x)$ are the i grad Chebyshev polynomials determined by the relations:

$$\begin{aligned} &T_0(x)=1 \\ &T_1(x)=x \\ &T_{n+1}(x)=2\cdot x\cdot T_n(x)-T_{n-1}(x);\quad n\geq 1 \end{aligned} \tag{14}$$

• *Mini-max approximation* or *optimal polynomial approximation* called that because the approximation polynomial is obtained after an optimization process by minimizing the maximum norm of the difference between function to be approximated and the polynomial approximation.

The functions with two variables are approximated by truncated Taylor expansion. The resulting approximated polynomials have the form:

$$\begin{aligned} &f_a(x_1,x_2)=f(0,0)+\sum_{k=1}^{N}\sum_{i=0}^{k}a_{ki}\cdot x_1^{k-i}\cdot x_2^{i} \\ &a_{ki}=\frac{1}{k!}\cdot C_k^i\cdot\frac{\partial^{k-i}f}{\partial x_1^{k-i}}\bigg|_{\substack{x_1=0\\x_2=0}}\cdot\frac{\partial^{i}f}{\partial x_2^{i}}\bigg|_{\substack{x_1=0\\x_2=0}} \end{aligned} \tag{15}$$

After approximation process, the approximated functions are decomposed in continued products. The one variable approximated function $f_a(x)$ become:

$$\begin{aligned} &f_a(x)=-p_0-q_0\cdot x+(1-x)\cdot\{-p_1-q_1\cdot x+ \\ &+(1-x)\{...\{-p_{N-1}-q_{N-1}x+(1-x)b_{N0}\}...\}\}= \\ &=h_0+g_1\{h_1+g_2\{h_2+...+g_{N-1}(h_{N-1}+g_Nh_N)...\}\} \end{aligned} \tag{16}$$

with p_i and q_i, $i=\overline{0,N}$, real parameters that may be determined from polynomial coefficients of approximated function.

The two variable functions, that have the form (15), are arranged in the following way:

$$\begin{aligned} &f_a^N(x_1,x_2)=\sum_{k=0}^{N}a_{k0}x_1^k+\sum_{k=1}^{N}a_{kk}x_2^k+x_1\sum_{k=2}^{N}a_{k,k-1}x_2^{k-1}+ \\ &+x_1^2\sum_{k=3}^{N}a_{k,k-2}x_2^{k-2}+...+x_1^i\sum_{k=i+1}^{N}a_{k,k-i}x_2^{k-i}+... \\ &+x_1^{N-1}\sum_{k=N}^{N}a_{k,k-(N-1)}x_2^{k-(N-1)}= \\ &+f_{a10}^N(x_1)+f_{a20}^N(x_2)+\sum_{i=1}^{N-1}f_{a1k}^N(x_1)\cdot f_{a2k}^N(x_2) \end{aligned} \tag{17}$$

with

$$f_{a10}(x_1)=\sum_{k=0}^{N}a_{k0}\cdot x_1^k;\ f_{a20}(x_2)=\sum_{k=1}^{N}a_{kk}\cdot x_2^k \tag{18}$$

$$\begin{aligned} &f_{a1k}^N(x_1)=x_1^k \\ &f_{a2k}^N(x_2)=\sum_{i=k+1}^{N}a_{i,i-k}x_2^{i-k},\ k=\overline{1,N-1} \end{aligned} \tag{18}$$

The functions $f_{a10}^N(x_1)$, $f_{a20}^N(x_2)$ and $f_{a2k}^N(x_2)$ are decomposed in continued products and she will have the forms corresponding to relation (16).

Therefore, for obtaining a translinear circuit which to realise a signal processing given by the one variable function, decomposed in the general form (16), the following set of equations must be implemented:

$$\begin{cases} z_N=h_N\cdot g_N \\ z_{i-1}=g_{i-1}\cdot(z_i+h_{i-1});\quad i=2,...,N \\ z=h_0+z_1 \end{cases} \tag{19}$$

The CMOS translinear expandable generic network that is implementing the equations (19) is shown in figure 2. It is very easy to see that in this network, all transistors, except T_{i5} transistor of the current sources, are saturated, $I_R<<I_F$ and therefore to good approximation we have:

$$\begin{aligned} &I_{Dij}=I_{Fij}=\frac{W_{ij}}{L_{ij}}\cdot I_{\Diamond}(V_{Gij})\cdot\exp\left(\frac{V_{GSij}}{V_T}\right) \\ &i=\overline{1,N},\ j=\overline{1,8}\ j\neq 5 \end{aligned} \tag{20}$$

For a minimum supply voltage, the current-source transistor T_{i5} will be non-saturated. Therefore, in accordance with decomposition technique described in section two (see figure 1.b.), the fictitious transistors $T_{i5}^{/}$ are added in order to account the non-saturation of these transistors. In figure 3 it is shown a section i of proposed network in which the added transistor $T_{i5}^{/}$ is shown dashed. From those presented in previous section, it follows that all shown network transistors can now be regarded as saturated.

Next, applying the Kirchoff low to the translinear loop T_{i1} - T_{i4} (see figure 3) it is obtained the following expression:

$$V_{GS_{i1}}+V_{GS_{i3}}=V_{GS_{i2}}+V_{GS_{i4}} \tag{21}$$

But from (20) we have:

$$V_{GS_{ij}}=V_T\cdot\ln\left\{I_{Dij}/\left[\frac{W_{ij}}{L_{ij}}\cdot I_{\Diamond}(V_{Gij})\right]\right\},\ j=\overline{1,4} \tag{22}$$

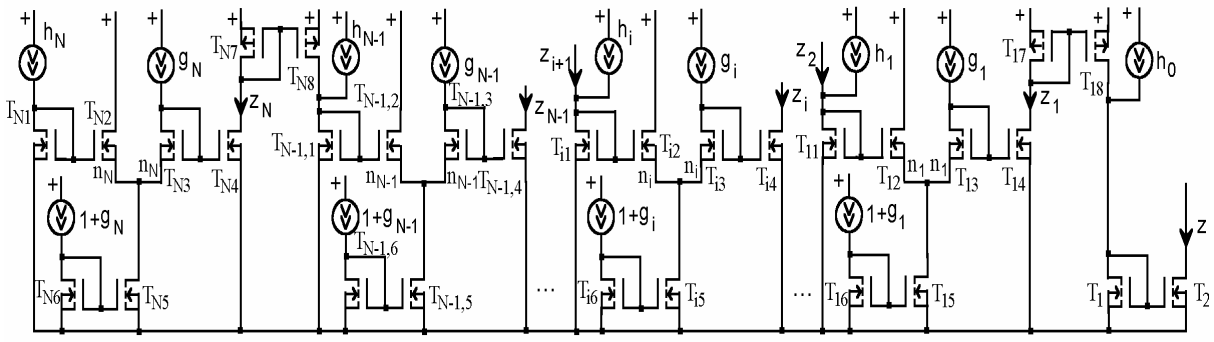

Figure 2. The CMOS translinear expandable generic network that implements the one variable polynomial approximated objective funtions.

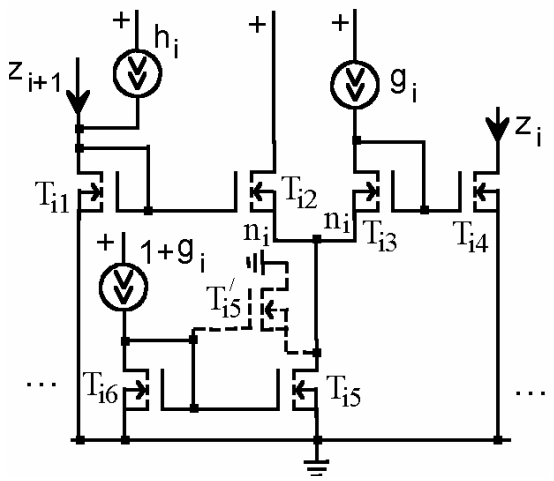

Figure 3. The i section of translinear generic network shown in figure 2.

So, the translinear loop equation becomes:

$$V_T \cdot \ln\left[\frac{I_{Di1}}{\frac{W_{i1}}{L_{i1}} \cdot I_{\Diamond}\left(V_{Gi1}\right)}\right] + V_T \cdot \ln\left[\frac{I_{Di3}}{\frac{W_{i3}}{L_{i3}} \cdot I_{\Diamond}\left(V_{Gi3}\right)}\right] = V_T \cdot \ln\left[\frac{I_{Di2}}{\frac{W_{i2}}{L_{i2}} \cdot I_{\Diamond}\left(V_{Gi2}\right)}\right] + V_T \cdot \ln\left[\frac{I_{Di4}}{\frac{W_{i4}}{L_{i4}} \cdot I_{\Diamond}\left(V_{Gi4}\right)}\right] \quad (23)$$

It can see that the oppositely connected transistor pairs T_{i1}, T_{i2} and T_{i3}, T_{i4} have the same gate voltage:

$$\begin{aligned} V_{GS_{i1}} &= V_{GS_{i2}} \\ V_{GS_{i3}} &= V_{GS_{i4}} \end{aligned} \quad (24)$$

It is follows that

$$\begin{aligned} I_{\Diamond}\left(V_{Gi1}\right) &= I_{\Diamond}\left(V_{Gi2}\right) \\ I_{\Diamond}\left(V_{Gi3}\right) &= I_{\Diamond}\left(V_{Gi4}\right) \end{aligned} \quad (25)$$

and the equation (23) becomes a classical translinear relationship independent of the body effect.

Assuming a constant rapport $W_{ij} / L_{ij}, i = \overline{1,N}$, $j = \overline{1,8}$ $j \neq 2$ and 3 for the adequate loop transistors and for the transistors T_{i2} and T_{i3} a size ratio multiplied by n_i, the equation (23) becomes:

$$\frac{I_{Di1}}{1} \cdot \frac{I_{Di3}}{n_i} = \frac{I_{Di2}}{n_i} \cdot \frac{I_{Di4}}{1} \quad (26)$$

and after we substitute the drain current with proper values, the equation will has the form

$$\left(z_{i+1} + h_i\right) \cdot g_i = I_{Di2} \cdot z_i \quad (27)$$

The drain current I_{Di2} can be evaluated from the second translinear loop of network section $T_{i3} - T'_{i5}$ and T_{i6}:

$$V_T \cdot \ln\left[\frac{I_{Di6}}{\frac{W_{i6}}{L_{i6}} \cdot I_{\Diamond}\left(V_{Gi6}\right)}\right] + V_T \cdot \ln\left[\frac{I_{Di3}}{\frac{W_{i3}}{L_{i3}} \cdot I_{\Diamond}\left(V_{Gi3}\right)}\right] = V_T \cdot \ln\left[\frac{I'_{Di5}}{\frac{W'_{i5}}{L'_{i5}} \cdot I_{\Diamond}\left(V'_{Gi5}\right)}\right] + V_T \cdot \ln\left[\frac{I_{Di4}}{\frac{W_{i4}}{L_{i4}} \cdot I_{\Diamond}\left(V_{Gi4}\right)}\right] \quad (28)$$

But

$$\begin{aligned} V_{GS_{i6}} &= V'_{GS_{i5}} \\ V_{GS_{i3}} &= V_{GS_{i4}} \end{aligned} \quad (29)$$

and thus

$$\begin{aligned} I_{\Diamond}\left(V_{Gi6}\right) &= I_{\Diamond}\left(V'_{Gi5}\right) \\ I_{\Diamond}\left(V_{Gi3}\right) &= I_{\Diamond}\left(V_{Gi4}\right) \end{aligned} \quad (30)$$

The second transliniar loop equation become:

$$\frac{1+g_i}{1} \cdot \frac{g_i}{n_i} = \frac{I'_{Di5}}{1} \cdot \frac{z_i}{1} \quad (31)$$

Applying the Kirchoff low in the connecting current source node yields:

$$I'_{Di5} = 1 - I_{Di2} \quad (32)$$

and from equation (31) results

$$\left(1 - I_{Di2}\right) \cdot z_i = \frac{1+g_i}{1} \cdot \frac{g_i}{n_i} \quad (33)$$

Substituting the z_i current expression from relation (27) yields

$$\left(1 - I_{Di2}\right) \cdot \frac{\left(z_{i+1} + h_i\right) \cdot g_i}{I_{Di2}} = \frac{1+g_i}{1} \cdot \frac{g_i}{n} \quad (34)$$

and the drain current I_{Di2} has the expression:

$$I_{Di2} = \frac{1}{\frac{1+g_i}{\left(z_{i+1} + h_i\right)} \cdot \frac{1}{n_i} + 1} \overset{n_i >> \frac{1+g_i}{(z_{i+1}+h_i)}}{\cong} 1 \quad (35)$$

It can see that for to obtain the relations (19) the multiplier of size ratio n_I must to come true the following relation:

$$n_i >> \frac{1+g_i}{\left(z_{i+1} + h_i\right)} \quad (36)$$

and in this way the relation (27) becomes:

$$\left(z_{i+1} + h_i\right) \cdot g_i \cong 1 \cdot z_i = z_i \quad (37)$$

Implementation of the functions that are not continued on the all definition interval but are continued on the subintervals that covered integer definition interval and are polynomial approximated on these subintervals

$$f_a^N\left(x\right) = \begin{cases} P_1 \text{ for } x \in [x_0, x_1) \\ \dots \\ P_i \text{ for } x \in (x_i, x_{i+1}) \\ \dots \\ P_n \text{ for } x \in [x_n, x_{n+1}) \end{cases}, \quad (38)$$

it is realised like in figure 4.

The network operates in a class A-B mode. It can see that the branch corresponded to the current source $x_i - x$ of the P_i section is in conduction only that the normalised variable x becomes grater than x_i. The oppositely connected branch (that corresponding to current source $x_{i+1} - x$) of the same section is designed in such way so that when come in conduction, she turn off the first branch (that corresponding to current source $x_i - x$). In this way the value of z will be given by P_I only for $x \in (x_i, x_{i+1})$. Unfortunately, this network can not operate at minimum supply voltage; she need a supply voltage about $3 \cdot V_P$ for good operating.

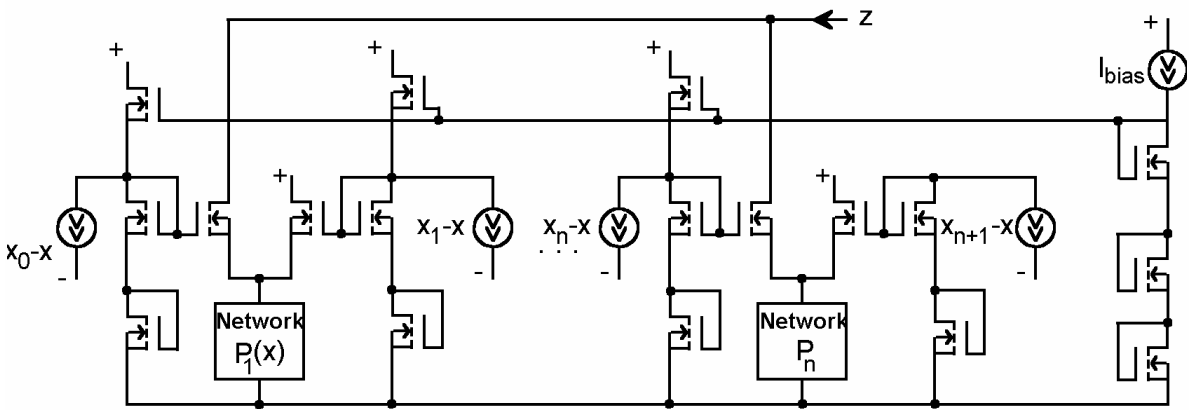

Figure 4. The network that is implementing polynomial approximated function that are not continued on the all definition interval but are continued on the subintervals that covered integer definition interval.

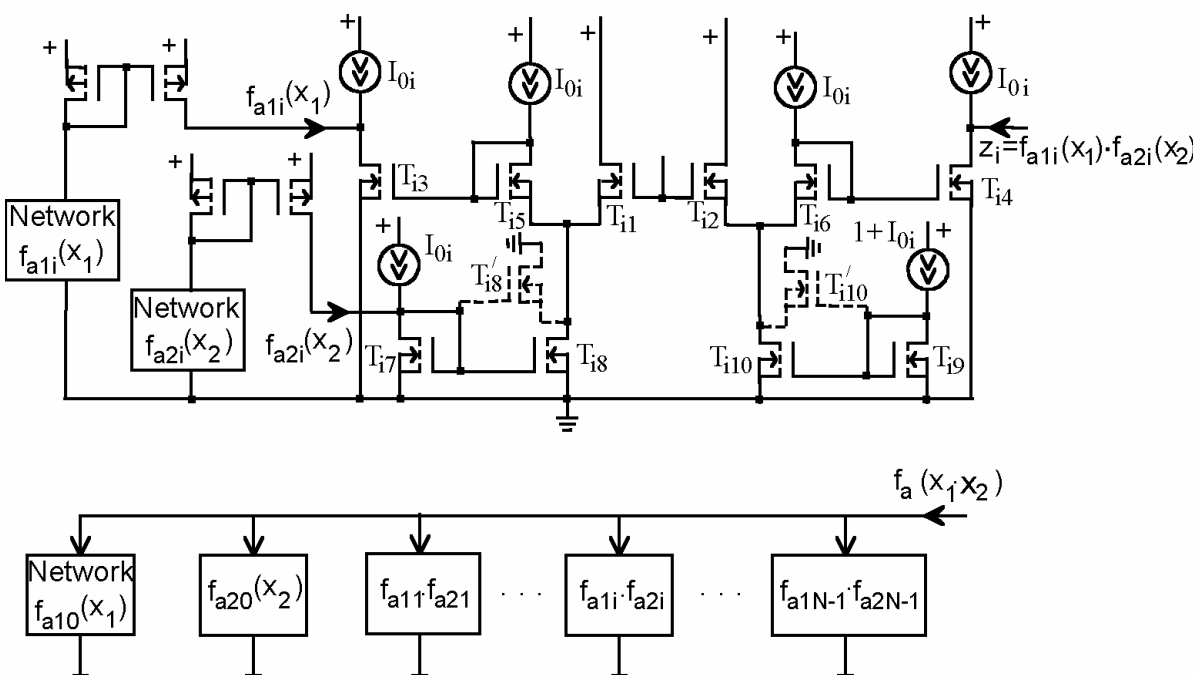

Figure 5. The network that is implementing the polynomial approximated two variable functions.

The two variables functions having the decomposition form (17) are implemented using the anterior presented networks for the one variable component functions (16) and supplementary networks that realised the appropriate products into the one variable polynomial function, as is illustrated in figure 5. The so obtained network is suitable for minimum voltage supply.

As in previous network (shown in figure 2) the tail current-source transistors are non-saturated. The addition of fictitious transistors $T_{i8}^{/}$ and $T_{i10}^{/}$ (shown in dashed line) allows all transistors to be regarded as saturated. The circuit are three translinear loops: T_{i1} – T_{i6}, next T_{i3}, T_{i5}, T_{i7} and $T_{i8}^{/}$ and finally T_{i4}, T_{i6}, T_{i9} and $T_{i10}^{/}$, which are immune from the body effect. Assuming equal-sized transistors for the translinear loops, applying the Kirchoff low to those and using the relation (22) for gate-source voltage, the loop equations become:

- for the first loop

$$\left(f_{a1i}(x_1)+I_{0i}\right)\cdot I_{Di1}\cdot I_{0i}=I_{0i}\cdot I_{Di2}\cdot z \tag{39}$$

- for the second loop

$$\left(f_{a2i}(x_2)+I_{0i}\right)\cdot I_{0i}=\left(f_{a1i}(x_1)+I_{0i}\right)\cdot I_{Di8}^{/} \tag{40}$$

with

$$I_{Di8}^{/}=f_{a2i}(x_2)+I_{0i}-I_{0i}-I_{Di1}=\\ =f_{a2i}(x_2)-I_{Di1} \tag{41}$$

- for third loop

$$I_{0i}\cdot\left(1+I_{0i}\right)=I_{Di10}^{/}\cdot\left(z_i+I_{0i}\right) \tag{42}$$

with

$$I_{Di10}^{/}=1+I_{0i}-I_{Di2}-I_{0i}=1-I_{Di2} \tag{43}$$

Eliminating I_{Di1} and I_{Di2} yields:

$$z_i=f_{a1i}(x_1)\cdot f_{a2i}(x_2) \tag{44}$$

The expressions for the drain currents of transistors T_{i1} and T_{i2} are

$$I_{Di1}=\frac{f_{a2i}(x_2)\cdot f_{a1i}(x_1)-I_{0i}^2}{f_{a1i}(x_1)+I_{0i}} \tag{45}$$

$$I_{Di2} = \frac{f_{a2i}(x_2)\cdot f_{a1i}(x_1) - I_{0i}^2}{f_{a2i}(x_2)\cdot f_{a1i}(x_1) + I_{0i}} \quad (46)$$

and relive that

$$\min_{x_1,x_2\in[-1,1]} \left[f_{a2i}(x_2)\cdot f_{a1i}(x_1)\right] > I_{0i}^2 \quad (47)$$

for a well operating of network.

We must pointed that the current-mode signals are natural for translinear circuits, but in the real-word systems voltage-signals are generally used and therefore voltage-current interfacing will be needed in practice.

3. CONCLUSION

The existing CMOS technologies provide ample opportunity to integrate entire systems on to a single integrated circuit. To date, the ability to integrate large digital systems has far outweighed the ability to integrate the analog systems. Future analog circuits will have to operate successfully at supply voltages slightly higher than the MOS threshold voltage. So, the suitable topologies for signal processing at such low values of supply voltages are the translinear circuits because are operating in current domain and in this way the very small voltage swings are avoided.

In this paper are presented three translinear topologies suitable for static and dynamic analog signal processing in mixed-signal chips fabricated in digital CMOS technology and operated at very low supply voltage. First, it is presented a expandable generic translinear network that is implementing the polynomial approximated one variable functions that are continue in entire definition domain. The minimum value of supply voltage required for this circuit is given by the sum of the MOS transistor threshold voltage and the drain-source saturation voltage. The second network that is presented in this paper is implementing the polynomial approximated one variable functions that are not continue in entire definition domain. This network is operating in a class A-B mode and unfortunately, she can well operate only at a value of supply voltage about $3\cdot V_P$. The last presented network is implementing the polynomial approximated two variable function. Like first network, this can operate at minimum value of supply voltage. Since the value of the supply voltage is low and the require of translinear principle to have a exponential I-V characteristic, the all transistors of these networks will operated in weak inversion. Therefore, bandwidth will be limited and the circuits will be sensitive to the threshold voltage matching.

For the previous presented networks will be developed algorithms so that to be integrated to the TLSS synthesis program. The TLSS is a program in C++ code, realized by me in period 1999-2000, which permits the automatic synthesis of translinear circuits. Also, will be studied the bandwidth, noise and errors due to transistors mismatching and will try to correct them.

REFERENCES

Doicaru, E. (1999). TLSS: A Structural Synthesis Program for the Translinear Integrated Circuits, *Proceedings of the 6th International Conference Mixed Design of Integrated Circuits and Systems*, page 405-409, Krakow, Poland.

Doicaru, E. (2000). Contribuţii la sinteza structurală a circuitelor analogice - teză de doctorat, Bucureşti.

Doicaru, E. (2002). Computer-Aided Synthesis of Transliniar Circuits by Using Polynomial Approximations, *Analele Universităţii din Craiova*, **nr.26, vol. II**, pag. 92-103, Craiova.

Enz, C.C., F. Krummenacher and E. Vittoz (1995), An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications, *IEEE Journal of Analog Integrated Circuits Signal Processing*, **Volume 8**, page 83-114.

Seevinck, E. (1988). Synthesis of TL Networks, *Analysis and Synthesis of Translinear Integrated Circuits,* Elsevier, page 69-132, Amsterdam.

Seevinck, E., E. Vittoz, M. Plessis, T. Joubert and W. Beetge (2000). CMOS Translinear Circuits for Minimun Supply Voltage, *IEEE Trans. Circuits Systems I*, **Volume no 46**, page 607-616.

Serrano-Gotarredona, T., B. Linares-Barranco and A.G. Andreou (1999), A general translinear principle for subthreshold MOS transistors, *IEEE Trans. On Circuits Systems II: Analog and Digital Signal Processing,* **Volume no 47**, no. 12, page 1560-1564.

Vittoz, E. (1994). Micropower techniques, *Design of VLSI Circuits for Telecommunication and Signal Processing*, Prentice Hall.

Vittoz, E. and J Fellrath (1997), CMOS analog integrated circuits based on weak inversion operation, *IEEE Journal of Solid-State Circuits*, **Volume SC-12**, page 224-231.