# DC-DC STEP-UP/DOWN CONVERTER USED TO DESIGN A SWITCHING POWER SUPPLY
## PART A: Mathematical Theory of DC-DC Step-Up/Down Converter controlled by MC34063 or µA78S40 Switching Regulator Control Circuits

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**Abstract –** The paper presents a DC-DC step-up/down converter used in switching power supply with monolithic switching regulator control circuits. The paper completely describes the design of the switching power supply starting with the simplified mathematical theory of the DC-DC step-up/down converter, getting on with the general description of MC34063 and µA78S40 operation modes and then with the mathematical theory of the DC-DC step-up/down converter in boundary conduction mode controlled by the switching regulation control circuits, the PSpice simulation of the whole switching power supply, a numerical example and ending with it's practical implementation. Conclusions about the efficiency of the switching power supply are drawn and some practical considerations are also included.

## 1. INTRODUCTION

The paper presents a DC-DC step-up/down converter and the switching power supply designed with it and with MC34063 and µA78S40 monolithic switching regulator subsystems. The DC-DC step-up/down converter makes the supply output voltage $V_{out}$ smaller, equal or greater then the supply input voltage $V_{in}$ without inverting the polarity of the output voltage compared to the polarity of the input voltage (as Buck-Boost converter does).

In modern switching power supplies design, the use of switching regulators becomes more pronounced over that of linear regulators because the size reduction in new equipments that require greater conversion efficiency and increased flexibility of output voltage compared with the input voltage. In addition, monolithic switching regulator subsystems represent a significant advanced in the ease of implementing highly efficient and yet simple switching power supplies [1], [2], [3].
Part A of this article treats mathematical theory of the DC-DC step-up/down converter and presents a general description of the switching regulator subsystems. In Part B the PSpice simulation of the whole switching power supply, a numerical example and its practical implementation, some practical considerations and the final conclusions are included.

## 2. BASIC OPERATION AND SIMPLIFIED MATHEMATICAL THEORY OF STEP-UP/DOWN CONVERTER

Fig.1 presents the basic configuration of a DC-DC step up/down converter as a combination between step-down (Buck) converter followed by step-up (Boost) converter. It employs a simple inductor L for the voltage transformation [4].

### 2.1. Basic operation of DC-DC step-up/down converter

Energy is stored in the inductor L (fig.1) during the time that transistors $Q_1$ and $Q_2$ are in the "on" state. Upon turn–off, the energy is transferred to the output filter capacitor and load forward biasing diodes $D_1$ and $D_2$. Note that during $t_{on}$ this circuit is identical to the basic step–up, but during $t_{off}$ the output voltage is derived only from the inductor and is with respect to ground instead of $V_{in}$.

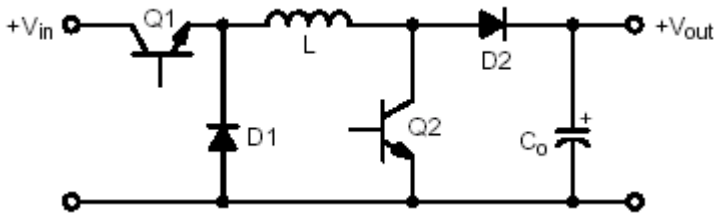


Fig.1. Basic configuration of DC-DC step-up/down converter

This allows the output voltage to be set to any value, thus it may be less than, equal to, or greater than that of the input. Current limit protection cannot be employed in the basic step–up circuit. If the output is severely overloaded or shorted, L or $D_2$ may be destroyed since they form a direct path from $V_{in}$ to $V_{out}$. The step–up/down configuration allows the control circuit to implement current limiting because $Q_1$ is now in series with $V_{out}$, as is in the step–down circuit.

### 2.2. Simplified mathematical theory of step-up/down converter

The symbols used in simplified mathematical treatment of DC-DC step up/down converter are: $V_{in}$ – input voltage, $V_{out}$ – output voltage, $t_{on}$– on-time of the output switching transistors $Q_1$ and $Q_2$, $t_{off}$ – off-time of $Q_1$ and $Q_2$, $T=t_{on}+t_{off}$ – total switching cycle time of $Q_1$ and $Q_2$, $D=t_{on}/T$ – duty ratio of switching transistors $Q_1$ and $Q_2$, L – output filter inductor, $i_L$ – inductor current, $I_{Lripple(p-p)}$ – ripple of current inductor $i_L$, $I_{LM}$ – maximum value of current $I_L$, $I_{Lm}$ – minimum value of current $I_L$, $C_0$ – output filter capacitor, $V_{ripple(p-p)}$ – ripple of output voltage $V_{out}$, $N=V_{out}/V_{in}$ - converter's equivalent transformer ratio.

Assuming that in fig.1 switching transistors $Q_1$ and $Q_2$ and biasing diodes $D_1$ and $D_2$ are ideal switchers, the output filter capacitor $C_0$ is infinite to keep the output voltage $V_{out}$ constant, the current through the inductor L is linear and the converter operates in the correct continuous conduction mode, simplified Kirchhoff equations during the switching transistor $Q_1$ and $Q_2$ on-time and off-time are:

- during the on-time $t_{on}$, when $Q_1$ and $Q_2$ are both on, $D_1$ and $D_2$ are both off:

$$V_{in} = L\frac{di_L}{dt} \cong L\frac{I_{Lripple(p-p)}}{t_{on}-0} = L\frac{I_{LM}-I_{Lm}}{t_{on}-0} \qquad (1)$$

- during the off-time $t_{off}$, when $Q_1$ and $Q_2$ are both off, $D_1$ and $D_2$ are both on:

$$0 = L\frac{di_L}{dt} + V_{out} \cong L\frac{I_{Lripple(p-p)}}{T-t_{on}} + V_{out} = L\frac{I_m-I_M}{T-t_{on}} + V_{out} \qquad (2)$$

From equations (1) and (2) above, the converter's equivalent transformer ratio N is:

$$N = \frac{V_{out}}{V_{in}} = \frac{t_{on}}{T-t_{on}} = \frac{D}{1-D} \qquad (3)$$

Equation (3) shows that using a step-up/down converter the non-inverting output voltage $V_{out}$ can be higher, equal or smaller than the input voltage $V_{in}$.

Basic simplified equations (1), (2) and (3) don't allow to design converter's components:

- the inductance L according to the current ripple $I_{Lripple(p-p)} = I_{LM} - I_{Lm}$ through the inductance L that can't be determined;
- the output capacitor filter $C_0$ according to the specified ripple $V_{ripple(p-p)}$ of the output voltage $V_{out}$ because it was assumed ideal $C_0 \to \infty$ when ideal $V_{ripple(p-p)}=0$.

## 3. GENERAL AND FUNCTIONAL DESCRIPTION OF MC34063 AND µA78S40 SWITCHING REGULATOR CONTROL CIRCUITS

The MC34063 series (fig.2.a) is a monolithic control circuit containing all the active functions required for DC-DC converters regulation.

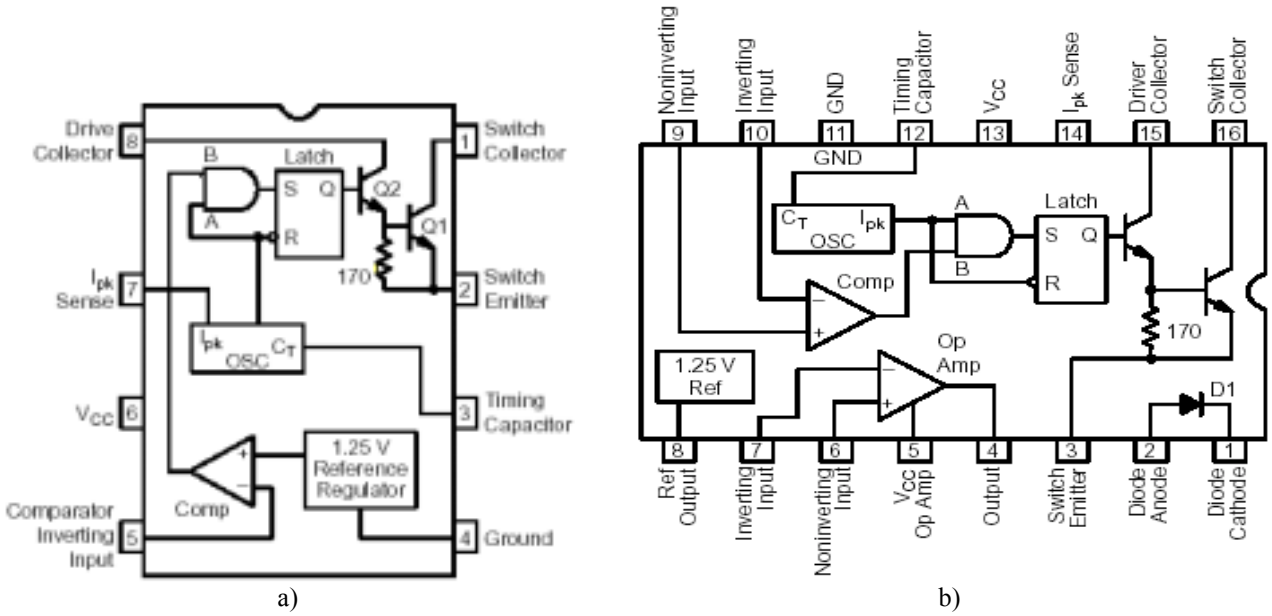
This device contains an internal temperature compensated reference of 1.25V, comparator, controlled duty cycle oscillator with an active peak current limit circuit, driver and a high current output switch. This series was specifically designed to be incorporated in step–up, step–down and voltage–inverting converter applications, but in this article it is used with step-up/down included in switching power supply application type. These functions are contained in an 8–pin dual in–line package.

The µA78S40 (fig.2.b) series is identical to the MC34063 with the addition of an on–board power catch diode and an uncommitted operational amplifier. This device is in a 16–pin dual in–line package, which allows the reference and the noninverting input of the comparator to be pinned out. These additional features greatly enhance the flexibility of this part and allow the implementation of more sophisticated applications. These may include series–pass regulation of the main output or of a derived second output voltage, a tracking regulator configuration or even a second switching regulator [5].

The easiest functional description follows the typical operation waveforms in fig.3.

*As long as the output voltage $V_{out}$ is bellow the nominal level* the comparator output presents a Logic "1" at the "B" input of the AND gate. The result is that during the charge time of the external timing capacitor $C_T$ as a Logic "1" at the "A" input of the AND gate will be also present. This causes the "Q" output of the latch to go to a Logic "1" enabling the driver $Q_2$ and the output switch $Q_1$ to be "on" and the output voltage increases to it's nominal level. One can observe in fig.3 that during the discharge of $C_T$ a Logic "0" at the "A" input of the AND gate will be present that causes the "Q" output of the latch to go to a Logic "0" disabling the driver $Q_2$ and the output switch $Q_1$.

The output voltage decreases during the discharge time of $C_T$ even it it's still necessary for the output voltage to increase to its nominal level. This is an inconvenient of MC34063 and µA78S40 operation modes that causes a small delay of milliseconds in reaching the nominal level.




a) b)

Fig.2. Functional block diagrams for: a) MC34063 b) μA78S40

In order to diminish it, the discharge time is internally set six times lower than the charge time.

*As long as the output voltage $V_{out}$ is above the nominal level* the comparator output presents a Logic "0" at the "B" input of the AND gate. This causes the "Q" output of the latch to go to a Logic "0" disabling the driver $Q_2$ and the output switch $Q_1$ and the output voltage decreases to and bellow the nominal output level. The whole functional operation starts again.

In fig.3 one can also observe that the nominal level never stay still; it always exists an output ripple voltage $V_{ripple(p-p)}$. In order to diminish it an output filter for the output voltage $V_{out}$ must be introduced in the schematics of the switching power supplies with MC34063 or μA78S40 switching regulator control circuits. Fig.3 also emphasizes a mixed control PWM and PFM of the output switch $Q_2$.

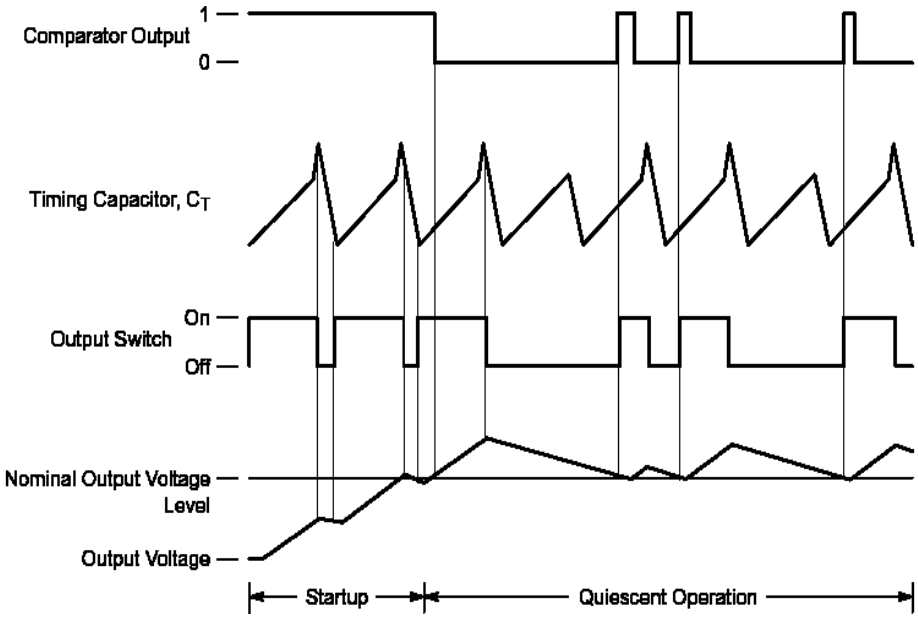



Fig.3. Typical operating waveforms

## 4. MATHEMATICAL THEORY OF DC-DC STEP-UP/DOWN CONVERTER CONTROLLED BY SWITCHING REGULATOR CONTROL CIRCUITS

The symbols added to those in chapter 2.2 that are used in mathematical treatment of DC-DC step up/down converter operating in boundary mode and controlled by MC34063 or μA78S40 monolithic switching regulator subsystems (fig.1) are as follows: $V_{FD1}$ –voltage drop on diode $D_1$, $V_{FD2}$ –voltage drop on diode $D_2$, $V_{satQ1}$ – voltage saturation of transistor $Q_1$, $V_{satQ2}$ – voltage saturation of transistor $Q_2$, $I_{L(pk)}$ – peak inductor current, $L_{min}$ –value of inductor L when the converter operates in boundary mode, $I_{pk(switch)}$ – peak switch current of $Q_1$, $I_{chg}$ – oscillator charge current, $I_{disch}$ – oscillator discharge current, $i_{C0}$ – current through the output capacitor filter $C_0$, $t_1$ – charge time of $C_0$, ESR – Equivalent Series

Resistance of $C_0$, $R_{sc}$ – limit resistor for $Q_1$ switch current, $R_L$ – load resistance.
The following mathematical theory was developped for the converter's boundary conduction mode in order to simplify the design steps. Then, choosing the inductor value L bigger than it's minimum value $L_{min}$ obtained for converter's boundary conduction mode,

the step-up/down converter will operate in the correct continuous conduction mode [1], [2].
The design steps are as follows:
*Step 1.* The output average voltage for DC-DC step-up/down converter is obtained from equation (3):

$$V_{out}=\frac{D}{1-D}\cdot V_{in}=\frac{t_{on}/t_{off}}{1-t_{on}/(t_{on}+t_{off})}\cdot V_{in}=\frac{t_{on}}{t_{off}}\cdot V_{in} \quad (4)$$

*Step 2.* The peak inductor current $I_{L(pk)}$ can be obtained writing the voltage Kirchhoff equation on fig.1during the time interval $t\in(0,t_{on})$ when transistors $Q_1$ and $Q_2$ are both on and biasing diodes $D_1$ and $D_2$ are both off, includind $V_{satQ1}$ and $V_{satQ2}$ transistors' saturation voltage. It can be observed that transistors $Q_1$ and $Q_2$ are not considered ideal switches:

$$V_{in}=V_{satQ1}+L\frac{di_L}{dt}+V_{satQ2}\cong$$

$$\cong V_{satQ1}+L\frac{I_{L(pk)}-0}{t_{on}-0}+V_{satQ2}$$

From equation above the peak inductor current $I_{L(pk)}$ is obtained:

$$I_{L(pk)}=\frac{V_{in}-V_{satQ1}-V_{satQ2}}{L}\cdot t_{on} \quad (5)$$

*Step 3.* During the time interval $t\in(t_{off},T)$ when transistors $Q_1$ and $Q_2$ are both off and biasing diodes $D_1$ and $D_2$ are both on the voltage Kirchhoff equation written on fig.1 also gives the peak inductor current $I_{L(pk)}$. Diodes $D_1$ and $D_2$ are not considered ideal switched because their voltage drops $V_{FD1}$ and $V_{FD2}$ are taking under consideration:

$$0=V_{FD1}+L\frac{di_L}{dt}+V_{FD2}+V_{out}\cong$$

$$\cong V_{FD1}+L\frac{0-I_{L(pk)}}{t_{off}-0}+V_{FD2}+V_{out}$$

From equation above the peak inductor current $I_{L(pk)}$ is obtained:

$$I_{L(pk)}=\frac{V_{out}+V_{FD1}+V_{FD2}}{L}\cdot t_{off} \quad (6)$$

*Step 4.* From equations (5) and (6) the ratio $t_{on}/t_{off}$ is obtained :

$$\frac{t_{on}}{t_{off}}=\frac{V_{out}+V_{FD1}+V_{FD2}}{V_{in}-V_{satQ1}-V_{satQ2}} \quad (7)$$

In equation (7) above the inductance L doesn't exist.
*Step 5.* The inductor current $I_L$ charges the output capacitor filter $C_0$ through diode $D_2$ during the time interval $t\in(0,t_{off})$. If the output voltage $V_{out}$ is kept constant then the load $Q^+$ during $t_{off}$ must be equal to the load $Q^-$ during $t_{on}$:

$$I_{chg}\,t_{off}=I_{dischg}\,t_{on} \quad (8)$$

The peak inductor current $I_L(pk)$ can be obtained from equation (8) and the waveforms of capacitor current $i_{C0}$:

$$\frac{I_{L(pk)}\,t_{off}}{2}=I_{out}(t_{on}+t_{off})\Rightarrow$$

$$\Rightarrow I_{L(pk)}=2I_{out}\left(\frac{t_{on}}{t_{off}}+1\right) \quad (9)$$

It can be observed that:

$$I_{L(pk)}=I_{pk(switch)}, \quad (10)$$

the peak inductor current $I_{L(pk)}$ being equal to the collector current of transistor $Q_1$ because the inductor L is put in the collector of $Q_1$.
*Step 6.* From equations (5), (9) and (10) the expresion $L_{min}$ of the inductor L when the step-up/down converter works in the boundary conduction mode is:

$$L_{min}=\frac{V_{in(min)}-V_{satQ1}-V_{satQ2}}{Ipk(switch)}t_{on} \quad (11)$$

*Step 7.* The ripple $V_{ripple(p-p)}$ of the output voltage $V_{out}$ can be calculated knowing $t_{on}$, $t_{off}$, $I_L(pk)$, $I_{out}$ and $C_0$. The charge time $t_1$ of output capacitor filter is experimentaly obtained from the waveforms of $i_{C0}$:

$$\frac{I_{pk}-I_{out}}{t_1}=\frac{I_{pk}}{t_{off}}$$

As the currents $I_{pk}=I_{L(pk)}=I_{pk(switch)}$ from equation above $t_1$ is:

$$t_1=\frac{I_{pk}-I_{out}}{I_{pk}}t_{off}, \quad (12)$$

during $t_1$ the current $i_{C0}$ can be written:

$$i_{C_o}(t)=\frac{I_{pk}-I_{out}}{t_1}t \quad (13)$$

and the output voltage ripple becomes:

$$V_{ripple(p-p)}=\frac{1}{C_0}\int_0^{t_1}i_{C0}(t)dt=\frac{1}{C_0}\cdot\frac{I_{pk}-I_{out}}{2}t_1 \quad (14)$$

From equations (12) and (14) results the final mathematical form of $V_{ripple(p-p)}$:

$$V_{ripple(p-p)}=\frac{(I_{pk}-I_{out})^2}{2I_{pk}C_0}t_{off} \quad (15)$$

As a practical observation, if a $V_{ripple(p-p)}$ error less than 5% is accepted and if $V_{out}>3V$, a simplier equation than (15) is accepted:

$$V_{ripple(p-p)}=\frac{I_{out}}{C_0}t_{on} \quad (16)$$

and equation (16) allows to dimension capacitor $C_0$.

## 5. PART A SUMMARY

The paper was split in Part A and Part B. Part A included a brief introduction, basic operation and simplified mathematical theory of DC-DC step-up/down converter, general and functional description of monolithic switching regulator control circuits MC34063 and μA78S40 and mathematical theory of DC-DC step-up/down converter controlled by them.

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