CMOS INTEGRATED NANOSTRUCTURE WITH IMPROVED TEMPERATURE DEPENDENCE

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Abstract: A new high precision superior-order curvature-corrected integrated nanostructure will be presented. In order to improve the temperature behavior of the circuit, a double differential structure will be used, implementing the linear and the superior-order curvature corrections. An original CTAT (Complementary To Absolute Temperature) voltage generator will be proposed, using exclusively MOS transistors biased in weak inversion for a low power operation of the integrated nanostructure, having two great advantages: an important reducing of the circuit silicon area and an improved accuracy (matched resistors being replaced by matched MOS active devices). The superior-order curvature-correction will be implemented by taking the difference between two gate-source voltages of subthreshold-operated MOS transistors, biased at drain currents having different temperature dependencies: $PTAT$ (Proportional To Absolute Temperature) and $PTAT^2$, respectively.

Keywords: temperature dependence, superior-order curvature-correction technique

1. INTRODUCTION

The design of the integrated nanostructures represents a theme of large actuality in the context of the analog and mixed VLSI circuit development. Evolution of the present MOS technologies towards nanometric dimensions amplifies the design difficulties, consequence of continuous degradation of quality for the model parameters associated to the active MOS devices. The fundamental laws which govern the functioning of elementary MOS structures, applicable in the case of classic design of VLSI, become, in many situation, inadequate for design of the modern integrated nanostructures. The incontestable advantages of circuits miniaturization (increasing of the functioning speed, reducing of power consumption and of minimum supply voltage, portability) are counterbalanced by the major difficulties of approaching of a project intended to implementation of high performance integrated nanostructures. Appears, in addition, the acute problem to find some mathematical models of which using implies a reasonable computing power and which permit an accurate analysis of the MOS nanostructures functioning, presenting - in the same time - continuity for all functioning regions. In this very restrictive context of nearness of dimensions for the active MOS devices to the technological limits, and of continuous alteration of quality for the associated model parameters, the development of some original circuit techniques, adapted to specificity of new restrictions imposed by evolution towards nanotechnologies, capable to compensate this degradation of performances, becomes a solution of large perspective.

In the very present and, in the same time, very restrictive context of optimizing the electronic structures performances for operating in the neighborhood of technological limits, the design of integrated nanostructures moves away from automatized area specific to any approaching of a technical project becoming, after successive overrunning of the technological barriers, art and inspiration, much more, possible, than systematic and rigorous treating of the fundamental concepts. The multiple applications of the integrated nanostructures and their actuality correlated with the remarkable advantages of such approaching, offer sufficient reasons for allocating an important time to design high precision integrated nanostructures.

Very important stages in applications such as A/D and D/A converters, data acquisition systems, memories or smart sensors, the integrated nanostructures with extremely small temperature dependence are derived from the traditional voltage reference circuits (Filanovsky, 1996), (Tham, 1995), (Vermaas, 1998), (Popa, 2001), presenting the great advantages of miniaturization and of compatibility with the newest CMOS nanotechnologies. The new proposed circuit represents a high precision integrated nanostructure designed for obtaining a very low temperature dependence for an extended temperature range. In order to fulfill these requirements, a superior-order curvature-corrected logarithmic core will be developed, based exclusively on subthreshold-operated MOS active devices, the original integrated nanostructure being design for low-voltage low-power operation.

2. THEORETICAL ANALYSIS

The new design of the high precision integrated nanostructure with improved temperature behavior starts from the gate-source voltage of a subthreshold-operated MOS transistor as a zero-order compensated temperature-dependent structure. The linear decreasing with temperature term from $V_{GS}(T)$ will be compensated by a complementary $CTAT$ voltage, obtained using an original approach based exclusively on MOS active devices. The logarithmic dependent on temperature term from $V_{GS}(T)$ will be cancel out by a proper difference between two gate-source voltages of MOS transistors biased at drain currents with different temperature dependencies.

2.1 The block diagram of the superior-order curvature-corrected integrated nanostructure with improved temperature behavior

The block diagram of the original proposed integrated nanostructure is presented in Fig. 1, containing:

- A zero-order curvature-corrected circuit (ZC);
- A double-differential structure (DDS), which represents the logarithmic core of the structure, implementing the linear and the superior-order curvature-corrections;
- An auxiliary current reference (ACR) for obtaining a $PTAT$ current and a current independent o temperature (in a first-order analysis);
- A current squarer (CSQ) for implementing a current with $PTAT^2$ dependence.

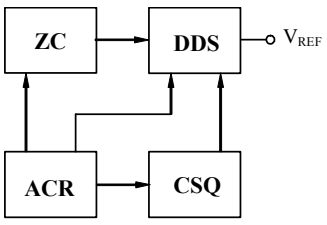

Fig. 1. The block diagram of the superior-order curvature-corrected integrated nanostructure

2.2 The zero-order curvature-corrected circuit (ZC)

The gate-source voltage of a MOS transistor working in weak inversion represents the simplest implementation in CMOS technology of a voltage generator with small negative temperature dependence. Considering a $PTAT^{\alpha}$ dependence of the drain current $I_D(T) = CT^{\alpha}$, α being a constant parameter, it results the following expression for the gate-source voltage:

$$V_{GS}(T) = V_{FB} + E_{G0} + \frac{V_{GS}(T_0) - V_{FB} - E_{G0}}{T_0} T + \\ + \frac{nkT}{q}(\alpha + \gamma - 2)\ln\frac{T}{T_0} \qquad (1)$$

where T_0 is the reference temperature. The first term is a constant term, the second one is a linear term, which will be compensated by a complementary linear dependent on temperature voltage and the last term models the nonlinearity of the gate-source voltage temperature dependence. This term will be compensated by a suitable logarithmic dependent on temperature voltage, also added to $V_{GS}(T)$.

2.3 The double-differential structure (DDS)

The logarithmic core of the superior-order curvature-corrected integrated nanostructure is represented by the DDS block (Fig. 2). Two important features could be achieved using this block: the linear and the superior-order curvature corrections.

The linear curvature correction

The linear curvature correction technique is necessary for compensating the linear decreasing with temperature term from (1). This complementary term will be obtained by using the difference between two gate-source voltages (V_{GS_2} and V_{GS_3} from Fig. 2, respectively). The implementation of a $PTAT$ voltage generator (T_2, T_3, T_5 and T_6) presents the important advantages of a strongly reduced silicon occupied area and of an improved accuracy obtained by replacing all the resistors from the circuit by MOS active devices. The linear curvature-correction voltage is represented by $V_{DB}(T)$, having the following expression:

$$V_{DB}(T) = V_{LIN}(T) = \left|V_{GS_3}(T)\right| - \left|V_{GS_2}(T)\right| \qquad (2)$$

resulting:

$$V_{LIN}(T) = \frac{nkT}{q}\ln\left[\frac{(W/L)_2(W/L)_6}{(W/L)_3(W/L)_5}\right] \qquad (3)$$

Choosing $(W/L)_2(W/L)_6 > (W/L)_3(W/L)_5$, the previous voltage will have a $PTAT$ variation, which will compensate the linear decreasing with temperature of $V_{GS}(T)$ from (1).

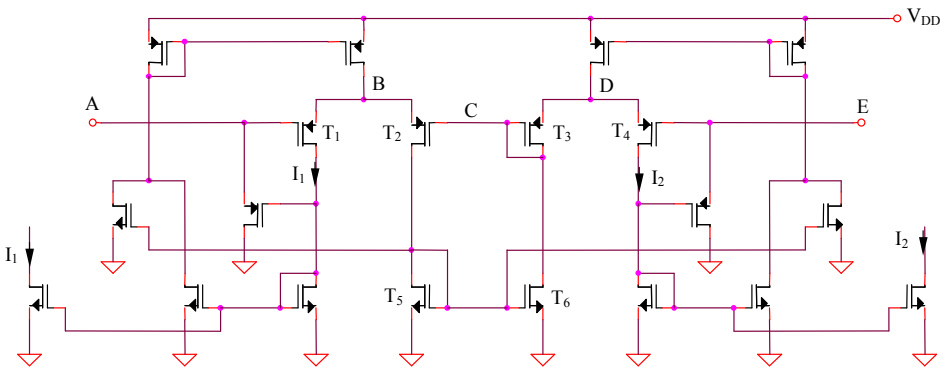

Fig. 2. The double-differential structure

The superior-order curvature-correction technique

The goal of this technique is to remove the logarithmic dependent on temperature term from (1) by inserting a circuit able to compute a voltage complementary to this term. The original method for implemented the superior-order curvature-correction is to consider the difference of gate-source voltages for MOS transistors biased at drain currents with different temperature dependencies. The superior-order correction voltages could be expressed as:

$$V_{SUP}(T) = V_{ED}(T) + V_{BA}(T) = \left|V_{GS_1}(T)\right| - \left|V_{GS_4}(T)\right| \quad (4)$$

Because T_1 is biased at a $PTAT$ current and T_2 works at a $PTAT^2$ current, considering the general relation (1) of the temperature dependence of the gate-source voltage, the superior-order correction voltage will have the following expression:

$$V_{SUP}(T) = -\frac{nkT}{q}\ln\frac{T}{T_0} \quad (5)$$

By a proper biasing of the MOS transistor from the zero-order curvature-corrected circuit, this term will compensate the logarithmic dependent on temperature term from $V_{GS}(T)$ (included in ZC block), resulting a theoretical zero value of the temperature dependence for the proposed superior-order curvature-corrected integrated nanostructure.

2.4 The superior-order curvature-corrected integrated nanostructure

The output voltage of the superior-order curvature-corrected integrated nanostructure will have the following general expression:

$$V_{REF}(T) = V_{GS}(T) + V_{LIN}(T) + V_{SUP}(T) \quad (6)$$

Supposing that the zero-order curvature-corrected circuit is biased at a $PTAT$ current and that the DDS block is biased at $PTAT$ and $PTAT^2$ currents, respectively (the generation of these currents will be further analyzed) and, additionally, that the linear correction is already made (imposing a relatively simple design condition to the circuits' parameters), the output voltage of the integrated nanostructure will have the following expression:

$$V_{REF}(T) = V_{FB} + E_{G0} + \frac{nkT}{q}(\gamma - 2)\ln\frac{T}{T_0} \quad (7)$$

The superior-order curvature-correction is achieved because of the usual value of the technological parameter $\gamma = 2$. By implementing both linear and superior-order curvature-corrections, the output voltage of the integrated nanostructure will have a theoretical zero value of the temperature coefficient:

$$V_{REF}(T) = V_{FB} + E_{G0} \cong 1.2V \quad (8)$$

The great advantages of the previous presented circuit are:

- The exclusively utilization of the MOS active devices, allowing an important decreasing of the silicon occupied area;
- The low-voltage operation of the circuit;
- The low-power operation obtained by a weak inversion of all MOS transistors from the circuit;
- The very small value of the temperature coefficient (theoretical zero) achieved by implementing two curvature-corrections, linear and logarithmical.

2.5 The auxiliary current reference (ACR)

The goal of this block is to generate two currents: I_0, which is, in a first-order approximation, independent on temperature and I_1, with a $PTAT$ variation. Any simple circuit using exclusively MOS active devices working in weak inversion could be used for implementing the auxiliary current reference.

2.6 The current squarer circuit

In order to obtain I_2 current with a $PTAT^2$ dependence for biasing the Double Differential Structure, a current multiplier using subthreshold-operated MOS transistors will be presented in Fig. 3. The relation between the circuit currents is $I_2 = I_1^2 / I_0$, resulting $PTAT^2$ variation for I_2 current (because I_1 current has a $PTAT$ variation).

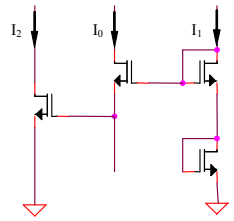

Fig. 3. The current squarer circuit

2.7 The second-order errors

The most important cause of the temperature dependence for the superior-order curvature-corrected integrated nanostructure is represented by the temperature dependence of the I_0 current, supposed to be independent on temperature, in a first-order analysis. Because this current is generated by a first-order curvature-corrected current reference, its real temperature dependence will be given by a logarithmical dependent on temperature term, similar to the last term from (1). So:

$$I_0(T) = A + BT\ln\left(\frac{T}{T_0}\right) \tag{9}$$

A and B representing constants with respect to the temperature variations. The nonzero temperature dependence of this current will be the cause of a not perfectly $PTAT^2$ variation of I_2 current, resulting:

$$I_2(T) = \frac{CT^2}{A + BT\ln\left(\frac{T}{T_0}\right)} \tag{10}$$

where C is also independent on temperature.

In order to estimate the error introduced in the output voltage of the integrated nanostructure expression by the nonzero value of the temperature coefficient for the reference current I_0, a more general expression of the temperature dependence for the gate-source voltage of a MOS transistor working in weak inversion will be developed:

$$V_{GS}(T) = V_{FB} + E_{G0} + \frac{V_{GS}(T_0) - V_{FB} - E_{G0}}{T_0}T + \\ + \frac{nkT}{q}(\gamma - 2)\ln\frac{T}{T_0} + \frac{nkT}{q}\ln\left[\frac{I_D(T)}{I_D(T_0)}\right] \tag{11}$$

representing a generalization of (1) for every temperature dependence of the drain current.

Considering that the drain current temperature dependence is $PTAT^2$, the gate-source voltage of T_4 transistor from Fig. 2 will be affected by an error quantitative evaluated by a linear term and a quadratic term:

$$\varepsilon(T) = \frac{nkT}{q}\left[\frac{nk}{qE_{G0}}(T - T_0) - \frac{nk}{2qT_0E_{G0}}(T - T_0)^2\right] \tag{12}$$

The linear term from (12) could be very easily removed by a small proper changing in the aspect ratios of T_2 and T_3 transistors from Fig. 2 (equivalent to a small variation of the $PTAT$ voltage necessary for the linear correction). The quadratic term from (12) will be concretized in an insignificant temperature coefficient of the superior-order curvature-corrected voltage reference.

3. CONCLUSIONS

A new high precision superior-order curvature-corrected integrated nanostructure has been presented. In order to improve the temperature behavior of the circuit, a double differential structure has been used, implementing the linear and the superior-order curvature corrections. An original CTAT voltage generator has been proposed, using exclusively MOS transistors biased in weak inversion for a low power operation of the integrated nanostructure, having two great advantages: an important reducing of the circuit silicon area and an improved accuracy (matched resistors being replaced by matched MOS active devices). The superior-order curvature-correction has been implemented by taking the difference between two gate-source voltages of subthreshold-operated MOS transistors, biased at drain currents having different temperature dependencies: $PTAT$ and $PTAT^2$.

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