2 X-BIT QCA ADDER

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Abstract: Considerable efforts had been made in studying QCA technology in order to achieve a strong and reliable computational paradigm that can enhance and even replace the already very expensive VLSI technologies. The aim of this paper is to present an adder that can be used in any type of future QCA processor. Furthermore we present some methods to connect this adder inside a nanoprocessor.

Keywords: Cellular automation, Adders, CAD/CAM models, Processor systems, Clocking, Computer Engineering, Quantization of charge

1. INTRODUCTION

Ever since John von Neumann invented Cellular Automata (CA) in the late 40's it had became an alternative in computing solutions. However, due to technological reasons, transistor based circuits were preferred. Nowadays, various investigators have pointed out the natural link between nanoscalar quantum systems and cellular automata architectures (Ferry a.o., 1996). Thus the gap between nanotechnology and cellular automata has been bridged.

Furthermore, the last few decades increase in the power of computation seems to have stopped, due to the fact that VLSI technologies have reached their physical limits. This has brought in the industry expensive technologies in order to obtain ultra-thin gate oxides or short channel effects. Under these circumstances QCA becomes attractive.

Some definitions for QCA technology are wellcome. We define a ***Quantum Cellular Automaton*** as being an array of quantum device cells in a locally interconnected architecture. For building the array of device cells we use ***Quantum Cells.*** A quantum cell is a device composed of several ***Quantum Dots***. We need to underline cell's bistability as it is the fundamental concept used in computation. Furthermore, the information we hold in such a cell needs to be transmitted to other cells in the cellular automaton and thus we need a mechanism of coupling for the neighboring cells. In order to achieve all these goals a cell composed of several quantum dots is considered. A quantum dot holds a predefined number of electrons.

Bistability and intercellular interaction are accomplished due to:

- Quantum confinement effects
- Coulomb interaction between electrons in the same cell
- Coulomb interaction between electrons in different cells
- Quantization of charge

We shall present only a few important advantages that QCA technology holds:

- Devices (quantum cells) used for this computational paradigm have dimensions of only a few square nanometers(Porod a.o.)
- It is estimated that 1-2nm quantum cells would function at room comparable temperatures (Timler a.o., 2002)
- Quantum cells use impulses as stimulus, and not current as the transistor does, therefore a drastic reduction in power consumption may result (Timler a.o., 2002)

- According to the estimations so far encountered the frequency at which such cells would function is of THz order (Hennesy a.o., 2001).

Using quantum pseudowires, quantum gates and quantum cellular and the QCA clocking scheme which utilizes 4 clocks we obtain several computational devices.(Lent a.o. Kummamuru a.o.,2005, Nicolae a.o., 2006).

2. THE ELEMENTARY ADDER

One of the most important devices inside a CPU is the adder. A sufficiently wide range of adders exist in the VLSI technology. However, in QCA and recent QCA nanoprocessors only one type of adder is used (Hennessy K.a.o., 2001, Niemier M. T., Kogge P. M., 1999) .

The structure of an elementary adder is very important to CPU development as the adder/subtracter is intensely used in computations such as those reminded above, namely addition and subtraction but also division and multiplication.

We mentioned before that computation in the QCA paradigm is carried out by using the majority gate, therefore our adder will use majority gates and inverters. The elementary adder is presented in Figure 1.

The colors represent the clocking of the QCA adder. There are four clocks, each clock signal being dephased by $\pi/2$, latching thus the signal passing through the quantum cells.

The QCA design of this adder is presented in Figure 2. This structure cannot be minimised in any other ways. However in the form presented here the computational power of the adder is not fully used. To support this argument we shall next present two sharp problems that such adder will present.

The first problem resides in the usage of the clocked adder pipeline. We observe that C_{out} is outputted

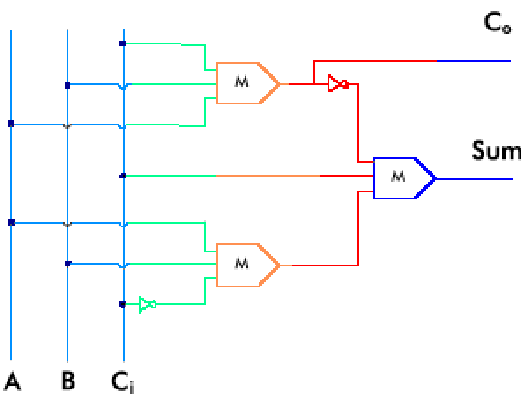

Fig. 1. Elementary Adder in QCA Technology

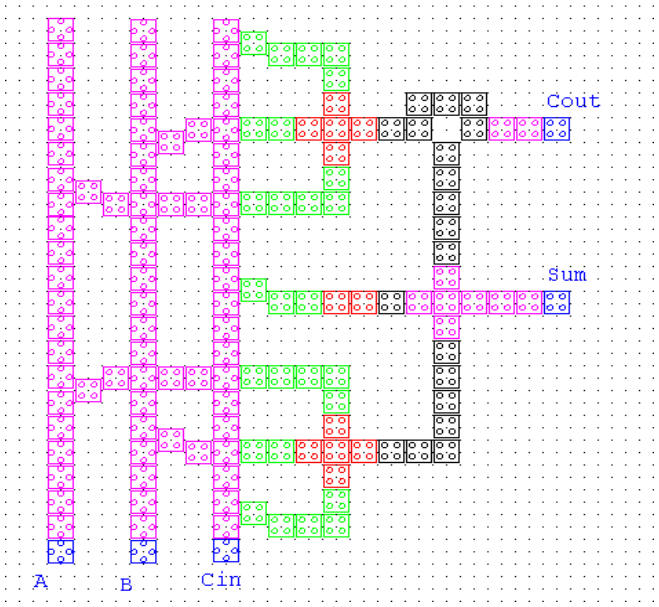

Fig. 2. Design using QCA cells of the Elementary Adder

from the circuit at the same time as Sum signal, that means on the first clock. However, Cout can be outputted much more early in the process, that means on the red clock, clock three. This is very important because inside a processor adders are cascaded in order to obtain the addition on several bits.

Even if this problem is solved there still remains one important problem that needs special attention. There was pointed out that in a very long pseudowire there may appear some faults in regarding signal passing. Therefore long wires are to be avoided. However if we imagine a 32 bit adder with each 1 bit adder cascaded to the following this problem certainly arises. Furthermore, even if this problem is solved the adder obtained would occupy a very large surface of the QCA chip, without using all the neccesarry space. Therefore these problems should be considered more carefully when implementing a nanoprocessor.

3. 2X BIT QCA ADDER

3.1. A First Improvement of the QCA Adder

There was previously said that C_{out} is available for outputing ever since clock three. This idea can be used in conjuntion with cascading adders. We take a simple example of cascading two adders. It would be unwise to waste time by carring Cout signal through clocks 3, 4 and 1 to be finally outputted. Therefore, as soon as clock 3 and at most clock 4 one can already use Cout as input signal Cin for the second adder. Figure 3 addresses this matter. If we cascade now two such devices we would obtain an adder on two bits which has a better response time than the cascaded first variant of the adder. Mainly this is due to the fact that on the two clocks we manage to save time resources that are next used for computational purposes for the next adder.The two improved cascaded adders are presented in figure 4.

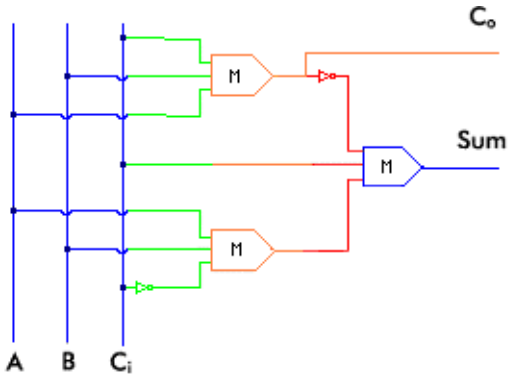

Fig. 3.Elementary adder with C_{out} outputted earlier

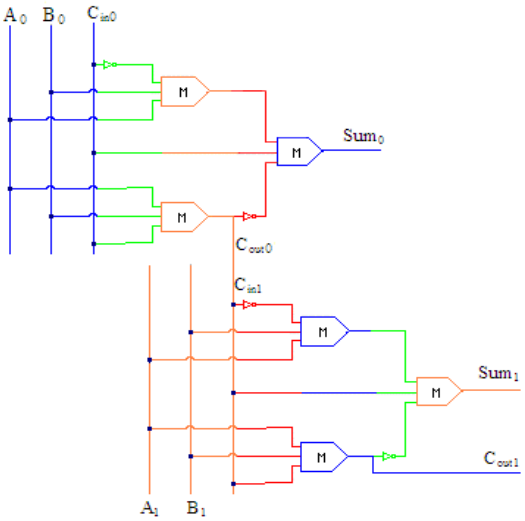

Fig. 4. Improved solution of two cascaded elementary adders

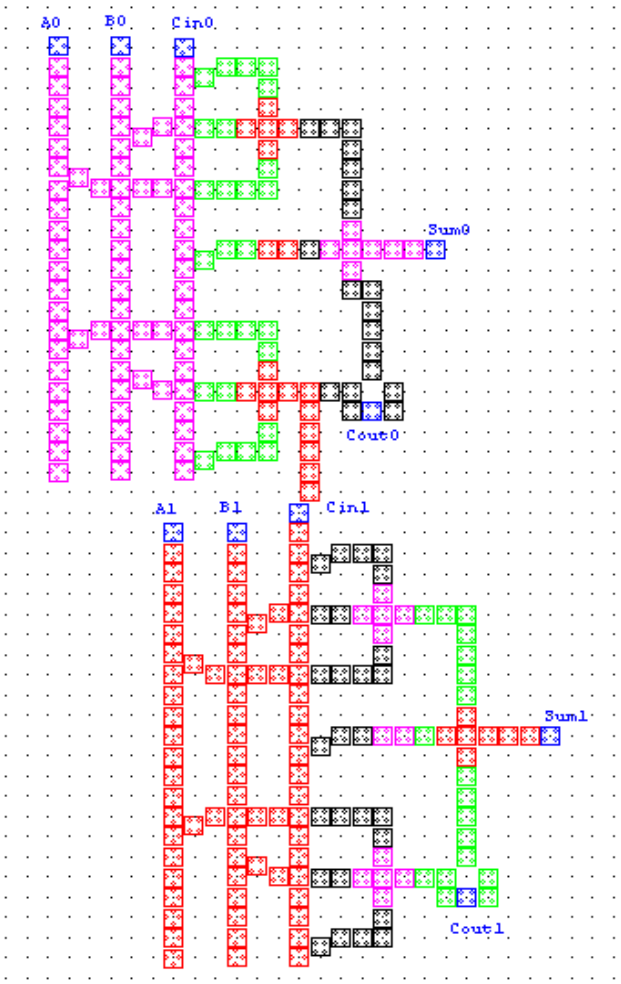

Fig. 5. The organisation of the two cascaded elementary adders

Based upon the principles presented above , we can create the QCA model of the cascaded adders. Although this improvement may seem more than enough to speed up an eventual processor, this kind of design still has some problems. The first problem arrising from this design can be observed at large adders, over 16 bits. Due to the fact that adders are cascaded together, a very long path from the first C_{in} to the last emerges. This long path can lead to inconsistencies in signal transmitting, large clocking circuits and all in all increases the production cost for such a device. Therefore a limited number of adders should be used. This comes in contradiction with nowadays neccesity to obtain 32-64 bits processors. Therefore one must make a compromise between a large processor and the use of a limited number of adders. An organisation with only two adders will be proposed.

Another problem is the disposal of clocking. Due to the fact that this particular organisation has a stair form, a very large portion of the adder is lost with clocking zones that will not produce any result, more than that they even don't contain any cells. This is contrary to our initial purpose of building ultradense circuits. Actually a considerable amount of space is wasted at this approach. One way to solve the problem would be to incorporate some additional logic (OR, AND, NOT operation). However even this solution is not the best as acces to outputs is very hard to obtain in this case. Therefore we should find a solution that is comparable in speed with the solution proposed above, and at the same time respects circuit's ultradense property.

3.2. A better solution

The solutions proposed before don't use all the flexibility provided by the QCA paradigm. In our case we could use a feed-back to obtain the same computational power but at a much more smaller scale. Instead of cascading our second adder on a left-to-right direction we shall do that vice-versa on a right to left direction. C_{out1} will be linked to C_{in0}, therefore obtaining a feed-back loop. This approach is presented in figure 6.

Based on this schematics we obtain the QCA configuration presented in figure 7.

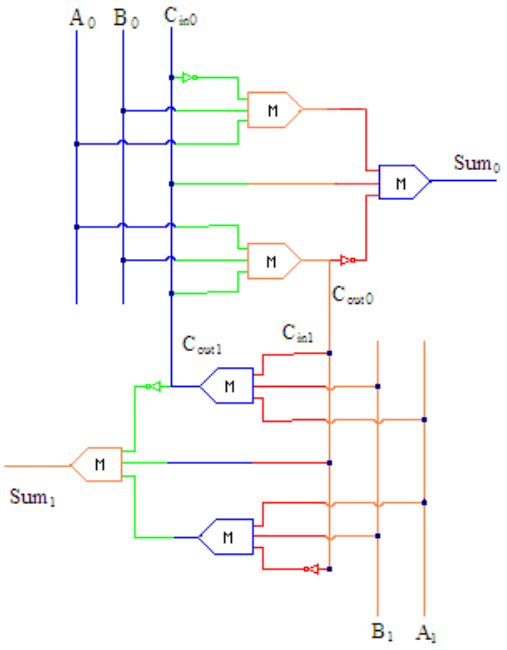

Fig. 6. Two adders in feed-back mode

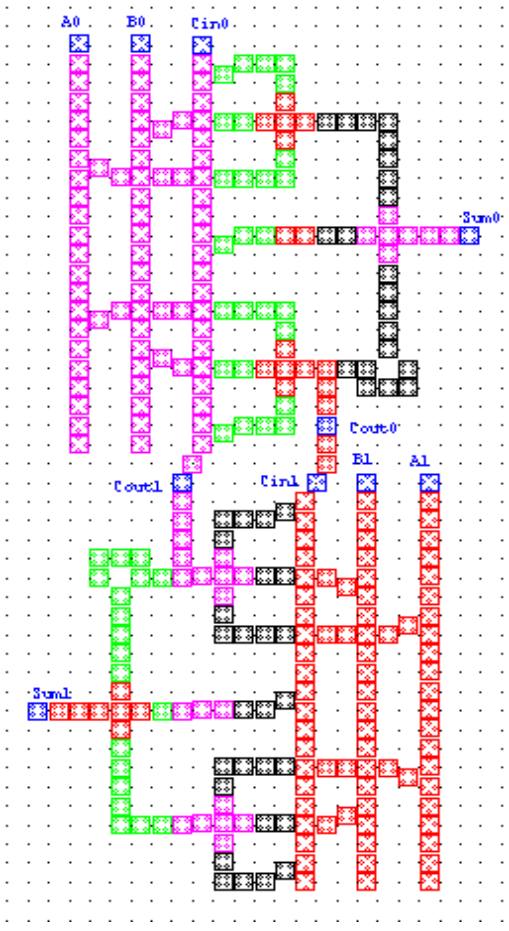

Fig. 7. The QCA organisation of the 2 feed-back adders

A crucial problem that arises at this step is the conflict between C_{out1} signals and C_{in0}, which take over the same line. We need to avoid this conflict and to do this one of the signals must be selected. Using a MUX induces an important delay on the circuit, slowing it considerably. Furthermore, in case of a 32-bit adder the signal C_{in0} will be used only once, therefore the usage of a MUX is not the best solution in this case. An actually better solution would be to inhibit C_{in0} after it is used.

An apparent problem of this design would also seem clocking zones. It can be observed that the clocking zones are not separated as good as in the previous models presented. However, the problem appears on clocks 2 and 4, which are 180˚ dephased, or more specifically, inverted.

4.CONCLUSION

If we were to compare a 32 bits adder built using the approach we will presented with a 32 variant of the same adder we can observe that the solution we shall next propose can be up to 1000 times smaller. Also considering that QCA cells will function at a frequency of THz order an important speed up can be observed. All in all an increase with several orders of the computational power is obtained.

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