DESIGNING, REALIZATION, AND TESTING OF A CURRENT CONDITIONING BOARD USED FOR PEBB CONVERTER CONTROL

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Abstract: The paper presents some problems related to the designing, realization and testing of a current conditioning board used for a PEBB power converter control. The recent achievements of power device technology, particularly related to the introduction of IGBT modules in power converters, provide the improvement of control performances. The current conditioning board is designed so as to interface with DSP and/or other type of evaluation boards. Therefore the board represents current signals like an electrical voltage proportional to the original signal. Moreover, the current conditioning board controls IGBT overcurrent protections. Finally one presents the waveformes recorded from different parts on the board.

Keywords: amplifiers, analog circuits, printed circuit testing, data acquisition.

1. INTRODUCTION

The Power Electronic Building Block (PEBB) concept refers to a general purpose power controller capable to realize numerous electrical conversion functions through software reconfiguration. It is also intended to facilitate greater modularity in power electronic systems. The Power Electronic Building Blocks (PEBB) are integrated modules containing power electronic devices used to switch large currents at high power levels to control, distribute, and process electric power. Figure 1 depicts a power module (Uraski *et al*., 2005):

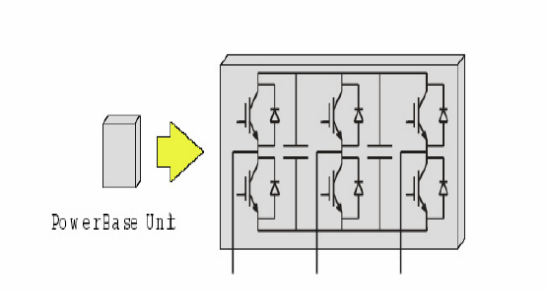

Fig.1. Power Electronic Building Block

The PEEB possible applications are imposed by the number of modules and by the control structure. The PEEB must satisfy the following features: modularity, flexibility, possibility to measure currents and voltages, low EMI emissions and low FEEDBACK noise from power blocks to control blocks.

2. DESIGNING AND REALIZATION OF A CURRENT CONDITIONING BOARD

The current conditioning board was designed to meet all requirements for a PEBB power converter control. Its roll is to interface with DSP, interface board and/or other type of evaluation board. Therefore this board represents current signals like an electrical voltage between Vmin and Vmax, e.g. 0….3V for DSP and 0….10V for dSPACE, which is proportional to the original signal.

The current conditioning should meet some requests owing to the features of converter and control systems (Garcia-Cerrada *et al*, 2004):

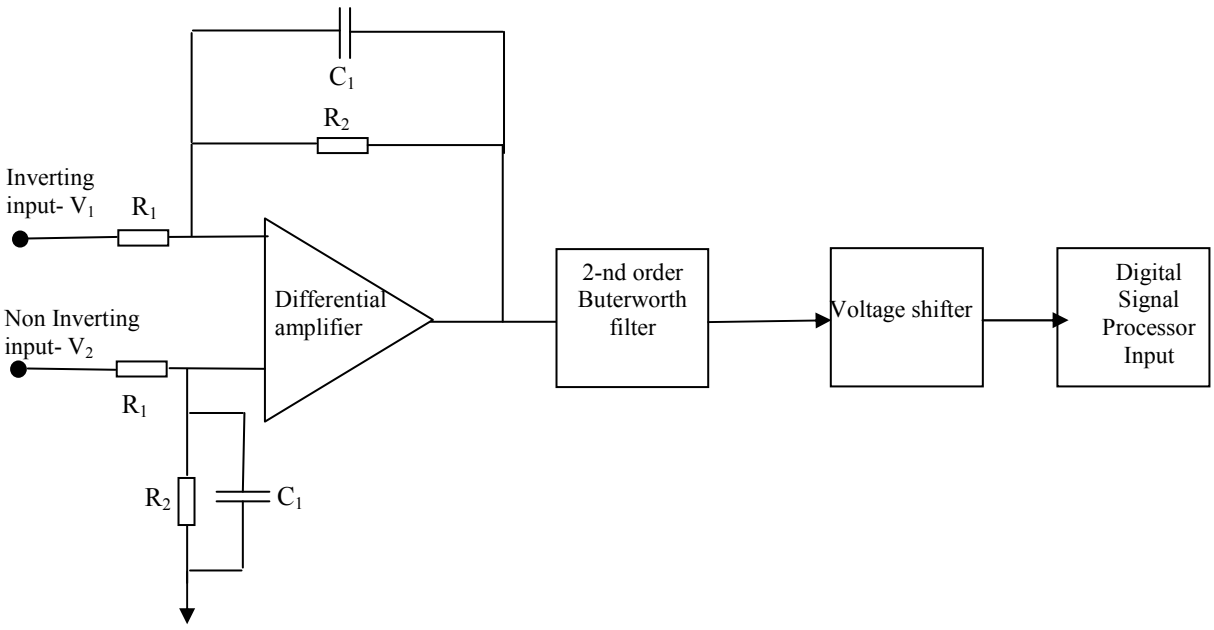

Fig. 2. The block diagram of a current channel

- one analog DSP connector with seven inputs;
- 100 mA input current for each channel;
- IGBT overcurents protection;
- seven BNC connectors for interface with dSPACE;
- 15 V DC power supply.

Figure 2 shows the block diagram of the basic configuration for a channel of the PEBB current conditioning board. The first block is a differential amplifier. The output voltage is proportional to the input differential voltage according to the following equation:

$$V_{out} = A \cdot V_d = A \cdot (V_1 - V_2) \tag{1}$$

Actually the output voltage is given by the following relations:

$$V_{out} = A_1 \cdot V_1 - A_2 \cdot V_2 \tag{2}$$

where A_1 is the gain corresponding to the inverting input and A_2 is the gain corresponding to the noninverting input.

Based on the following system:

$$\begin{cases} V_{CM} = \dfrac{V_1 + V_2}{2} \\ A_c = A_1 + A_2 \\ A_d = A_1 - A_2 \\ V_{DM} = \dfrac{V_1 - V_2}{2} \end{cases} \tag{3}$$

the output voltage at the differential amplifier is:

$$V_{out} = A_d \cdot V_{DM} \left[1 + \frac{V_{CM}}{V_{DM} \cdot CMRR} \right] \tag{4}$$

where:
- VCM is the common mode voltage;
- ACM is the common mode amplification;
- ADM is the differential mode amplification ;
- VDM is the differential mode voltage;
- CMRR is the Common Mode Rejection Ratio.

The following block is a Butterworth second order low pass filter realised in a Sallen-Key topology. The Butterworth low-pass filter provides maximum passband flatness. Therefore, a Butterworth low-pass is often used as anti-aliasing filter in data converter applications where precise signal levels are required across the entire passband. The filter components are mounted on a hoof to provide it with the ability to change the band if necessary (Chakraborty, 2005). The Butterworth filter for this application must have the cut off frequency equal to 5 kHz.

The transfer function of a Butterworth second order low pass filter is:

$$H_2(s) = \frac{1}{1 + a_2 \cdot s + b_2 \cdot s^2} \tag{5}$$

where a_2 and b_2 are the second order filter coefficients.

The quality factor Q is an equivalent design parameter to the filter second order and represents the pole quality. For low pass- filter it is defined by the following relation:

$$Q = \sqrt{b_2} / a_2 \tag{6}$$

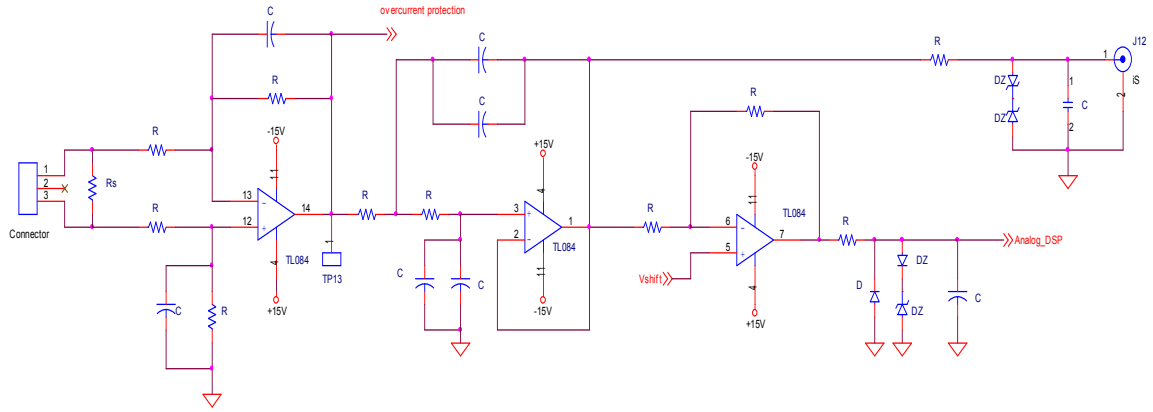

Fig. 3. An OrCAD schematic of the current channel

The DSP imposes the analog input range of its analog inputs, typically:

$$0 < V_{INPUT\_DSP} < V_{REF} \qquad (7)$$

The board contains seven signal channels, six for IGBT currents and one for dc-link current. In the figure 3 there is presented a current channel realized with a dedicated program (Salzar and Joos, 2006). The reference voltage V_{REF} is provided by an external circuitry or, for some DSPs, it is internally generated. When V_{REF} is externally generated, special care must be given to have V_{REF} as noise free as possible. Any noise on the V_{REF} voltage will be directly transferred to the digital result of conversion.

Usually, the analog inputs to be converted are not in the range [0, V_{REF}]. In addition, some analog quantities must be filtered to avoid the aliasing effect. Consequently, an analog conditioning circuitry must be used. For bipolar analog signals, a $V_{REF}/2$ voltage shift must be performed as depicted by figure 4.

3. TESTING OF A CURRENT CONDITIONING BOARD

The experimental determinations focused on the recording of voltages waveforms from the current conditioning board. The output signal for DSP has values between (0…+3V) according with data sheet and for dSPACE has values between (-10 V…+10 V).

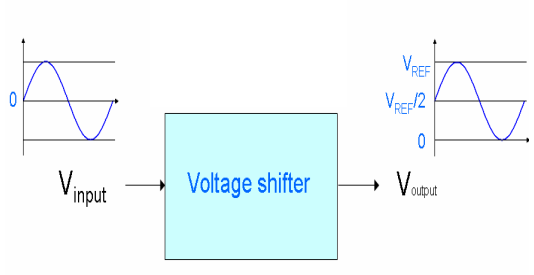

Fig. 4. Analog conditioning

It were been made following tests (Marchesoni, and Vacca, 2007):
- the Offset test;
- the DC gain test;
- the bandwidth test with Butterworth filter;
- the differential amplifier test.

1) Offset test

The major cause of the offset consists in the fact that the operational amplifiers are realized with components that require polarization currents and voltages.

The tests were made for each channel. The inputs channels were brought in the short circuit state and the output voltage was measured for each channel. Table 1 presents the obtained offset values.

2) DC gain test

DC gain tests were made to check the gain of differential amplifiers from the channel input. Therefore it was necessary to measure the input and differential amplifiers output voltage (Nedic and Lipo, 2006).

Table 2 presents the inverted output voltages of the differential amplifiers for a fixed input voltage. In this case the input voltage was 1.1 V.

3) The Bandwidth test with Butterworth filter

This test was necessary in order to check the bandwidth for the low pass filters mounted downstream the differential amplifier.

Table 1 The offset values

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7
0.0220 V	0.0180 V	0.0170 V	0.0097 V	0.0151 V	0.0057 V	0.0064 V

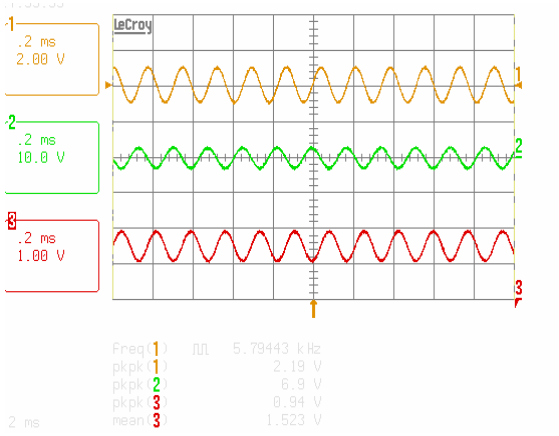

Fig. 5. The recorded waveforms corresponding to the filter test

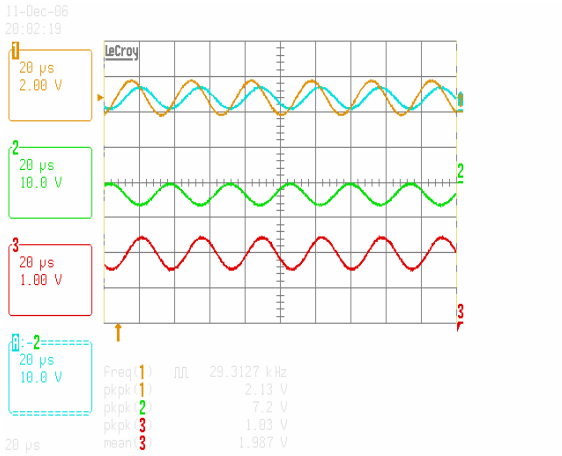

Fig. 6. The recorded waveforms corresponding to the differential amplifier bandwidth

Table 2. DC gain test

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7
-5.04 V	- 5.00 V	-4.97 V	- 4.98 V	- 4.95 V	-4.97 V	- 4.97 V

Fig. 5 depicts the recorded waveforms of the input channel (1), along with the recorded waveforms of the dSPACE output channel (2) and of the DSP output channel (3). The peak to peak value of the input signal amplitude was 2.2 V meanwhile the peak to peak value of the operational amplifier output signal was 10 V due to the amplifier gain (4.454 value). The filter response was approximately 7.07 V (peak to peak value) corresponding to the 5.8 kHz bandwidth.

4) The differential amplifier test

The differential amplifier test was necessary in order to check the bandwidth of the differential amplifier (Ghosh and Narayanan, 2007). Fig. 6 depicts the recorded waveforms of the input channel (1), along with the recorded waveforms of the differential amplifiers output channel (2) and of the DSP output channel (3). The peak to peak value of the input signal amplitude was 2.2 V meanwhile the peak to peak value of the operational amplifier output signal was 7.2 V.

Based on the recorded waveforms from fig. 6, one can determine the differential amplifier bandwidth which in this case is 30 kHz .

4. CONCLUSIONS

The current conditioning board was realised according to the PEBB power converter applications. The development of PEBB imposes small errors for signal acquisition.

Difference between signals measured value and imposed value are small for this applications and will not affect the DSP and dSPACE output signals. The signals measured in all tests conditions (the Offset test, the DC gain test, the bandwidth test, andthe differential amplifier test) shows a good agreement between the designing stage and the final utilisation.

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