A TOOL FOR TESTING THE SRAM MEMORIES

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Abstract: This paper presents a tool for testing the SRAM memories with a maximum capacity of 526kwords x 8bits. The permitted working modes, the chosen clock frequencies, the blocking of the scheme in case of a fault and the possibility of visualizing the address of the word which contains the fault, make this tool a most useful instrument for the SRAM memories users.

Keywords: block, SRAM, memory, clock, testing, fault.

1. INTRODUCTION

The SRAM memories (Wakerly, 2002) are very used to store the data in small microprocessor systems of "embeded" type, in application such as mobile phones, toasters, rotisseries, etc. They are made by various technologies, at different sizes and speed. The SRAMs with the greatest capacity are those realized in CMOS technology. Although they are not standardized from manufacture code point of view, the SRAMs are often identical in pins signals distribution. Moreover, various kinds of SRAMs having capacities between 8Kwords x 8bits and 512Kwords x 8 bits are almost perfectly consistent from this point of view.

The testing of this memories range supposes the allocation of a socket with 32 pins for the SRAM memory and also a careful study of the pins compatibility from a memory type to another one. Next, we show the testing a Hitachi memory of 128Kwords x 8bits.

2. THE SCHEME DESCRIPTION

As it is shown in fig. 1, the scheme is made of the following blocks:

- the clock generators block;
- the counters block;
- the 3-state buffer block;
- the SRAM block;
- the comparator block;
- the fault memorizing block;
- the signal block;
- the supply block.

2.1. The Clock Generators Block

The clock generators block (Blakeslee, 1988; Millman and Grabel, 1991), fig. 2, has the role of giving the clock for synchronizing the whole scheme and it presents two working modes: automatic and manually.
If the S1 switch is not operated (see fig. 2 and fig. 11), the generator gives manual clock at each K2 push-button pressing.
If the S1 switch is operated, the generator works in automatic mode on two possible frequencies (2Hz and 123KHz) which can be selected by acting the S2 switch (see fig. 2 and fig. 11).

The NOR gate allows the clock and the whole scheme blocking in two cases: the ending of the testing cycle for the whole memory (1 logic on B21 terminal) or the detection of a fault memory location (1 logic on B24 terminal).

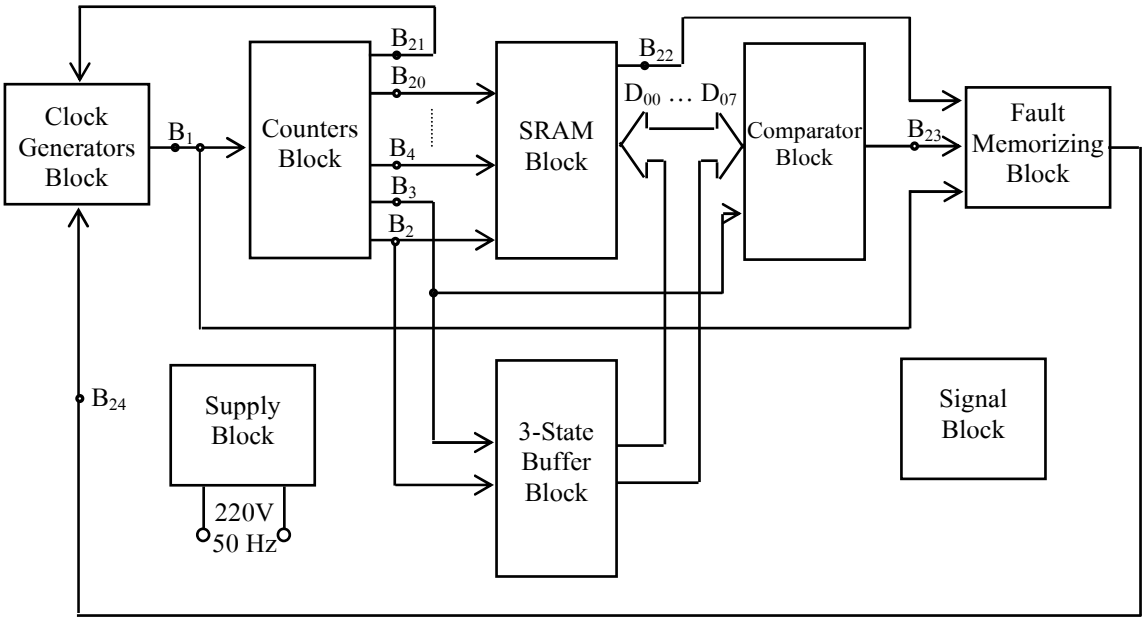

Fig. 1. The block scheme

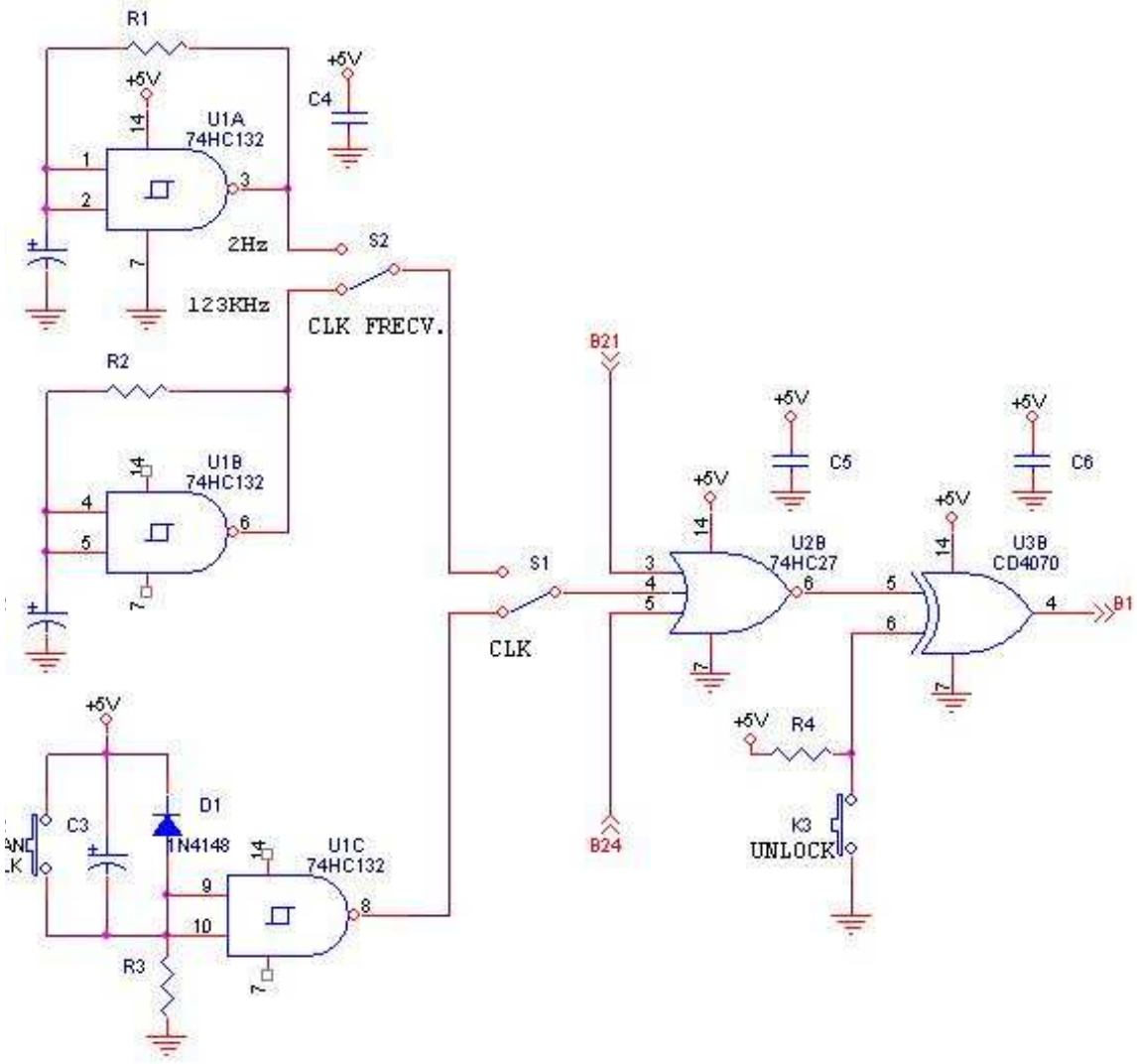

Fig. 2. The clock generators block

The K3 push-button allows the clock and the whole scheme unlocking if it is wanted to continue the memory testing after detecting a fault.

2.2. The Counters Block

The counters block (Filipescu,2002; Wakerly, 2002), fig. 3, is made of two 12-stage binary ripple counters, series connected.

From the 24 outputs only the first 20 ones are used (B2 … B21 terminals) as following:
- B2 and B3 terminals together with B1 terminal (CLK) assure the necessary signals to establish the work modes of the circuit: writing, reading, testing at 0 or 1, etc.
- B4 … B20 terminals correspond to the addresses A0 … A16 of the tested SRAM memory HM628128 and make possible the successive selection to test each group of 8 memory locations in 131,072 groups.
- B21 has the value 1 logic at the end of a testing cycle blocking the clock and the whole scheme.

The K1 push-button (reset) allows to bring the counters at 0 and to initialize the scheme.

2.3. The 3-State Buffer Block

The 3-state buffer block (Millman and Grabel, 1991), fig. 4, is made of an octal 3-state buffer 74HC244 and a XOR gate.

The XOR gate permits the application of the signal, presented in fig. 10g, to the 8 inputs (Ai) of the buffer.

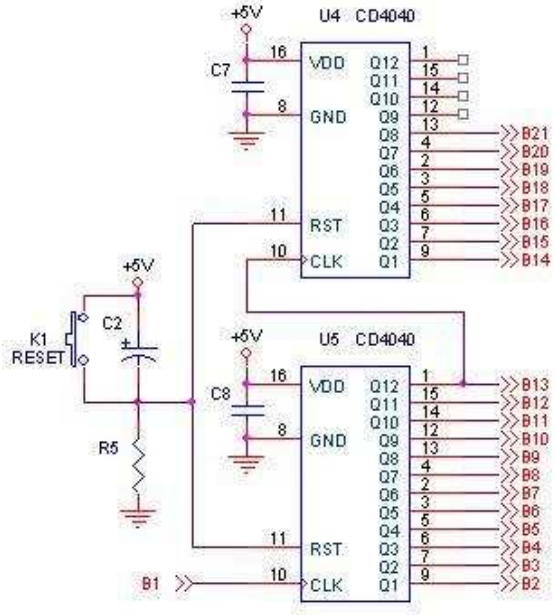

Fig. 3. The counters block

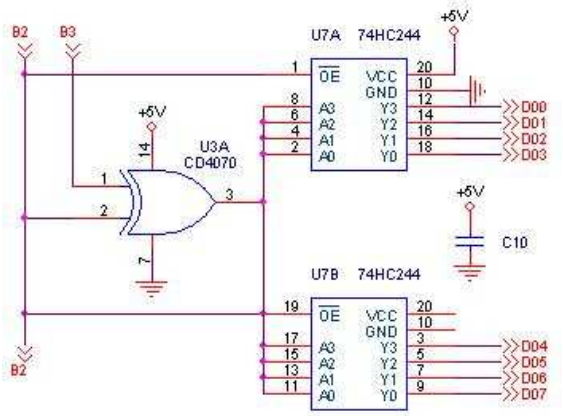

Fig. 4. The 3-state buffer block

This signal will have a certain logical value in the t_1-t_2 interval (fig. 10) when $\overline{OE} = 1$ and the buffer is in HZ state and it mentains the same logical value in the t_2-t_3 interval when $\overline{OE} = 0$ and takes place the data transfer from the buffer input to its output.

2.4. The SRAM Block

The SRAM block (Wakerly, 2002), fig. 5, is made of the SRAM CMOS high speed memory HM628128, having a capacity of 131,072words x 8bits and a XOR gate used like an inverter.

The signal applied to B2 terminal assures the writing and reading cycles of the memories as shown in the diagram in fig. 10e.

2.5. The Comparator Block

The comparator block, fig. 6, is formed by the integrated circuit 74HC688, an 8-bits magnitude comparator which offers an 1 logic at its output when the word of 8 bits read from the memory differs from the 8 bits word applied to the memory in the writing cycle.

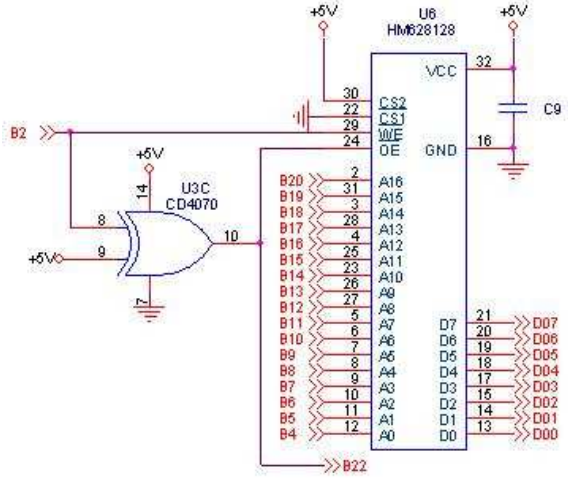

Fig. 5. The SRAM block

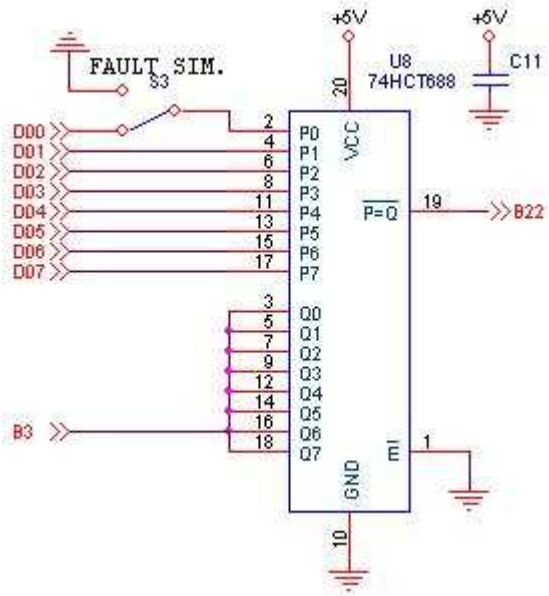

Fig. 6. The comparator block

The S3 switch (fault simulation) allows checking the comparator and the whole scheme correct working if there is a simulated fault at 1 bit of a memory octet.

2.6. The Fault Memorizing Block

The fault memorizing block (Filipescu, 2002), fig. 7, consists of a D-type flip-flop to whose input is applied the comparator output signal, B23 terminal, and to the clock input is applied the signal shown in the diagram in fig. 10h.

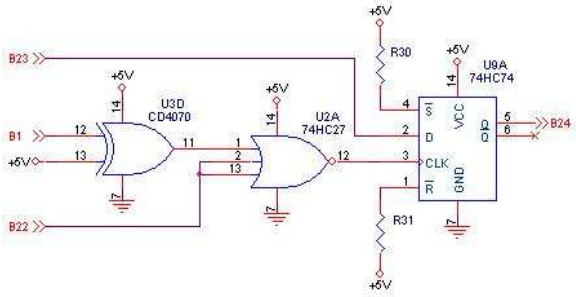

Fig. 7. The fault memorizing block

This signal is obtained with the help of a XOR gate used like an inverter and of a NOR gate.

It was desired that the increasing front of the clock should "fall" in the middle of the reading interval of the information in the memory, the moment in which the information is stable.

2.7. The Signal Block

The signal block, fig. 8, is formed by 24 signal circuits with LED.

Excepting the first signal circuit, fig. 8a, which shows the presence or the absence of the scheme voltage supplies, the 23 circuits, fig. 8b, need negligible control current, allowing the undisturbed working of the circuit at whose outputs they are placed.

2.8. The Supply Block

The supply block, fig. 9, contains, mainly, a 3-terminal positive voltage regulator which gives 5V at 1A to supply the whole tool.

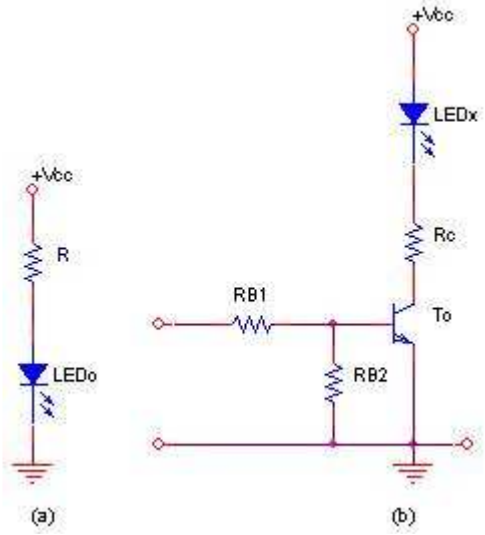

Fig. 8. The signal block

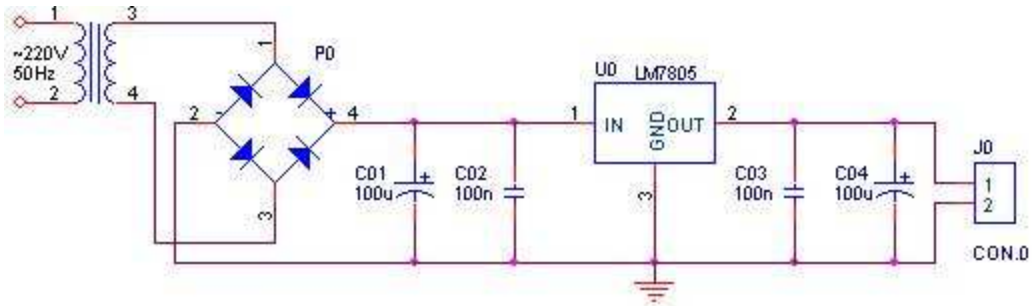

Fig. 9. The supply block

3. THE SCHEME WORK DESCRIPTION

The counters and the whole scheme initialization takes place by C2 in the moment the voltage supply is coupled, fig. 3, or by acting the K1 push-button (reset). From this moment, the scheme begins to work in accordance with the signal diagram in fig. 10.

The clock impuls frequency in automatic testing mode can be of 2Hz or 123KHz. The 2Hz frequency has been chosen for an easy observation of the testing process while the work frequency of 123KHz leads to a reasonable period of about 4 seconds for a complete testing cycle.

The adopted principle in designing this tool was that, once addressed an octet of memory locations, these are successively tested at 0 and 1 logic.

So, in the 0-t_1 interval, fig. 10, to the 8 inputs (Ai) of the 3-state buffer is applied 0 logic (Ai=0, fig. 10g) and as $\overline{OE}(B2) = 0$, the word D7 … D0 = 0 … 0 is applied to the corresponding I/O ports of the SRAM memory being in writing mode ($\overline{WE} = 0$, diagram in fig. 10d).

In the t_1-t_2 interval the 3-state buffer goes into HZ state ($\overline{OE} = 1$, fig. 10f) and the SRAM memory goes into the reading mode.

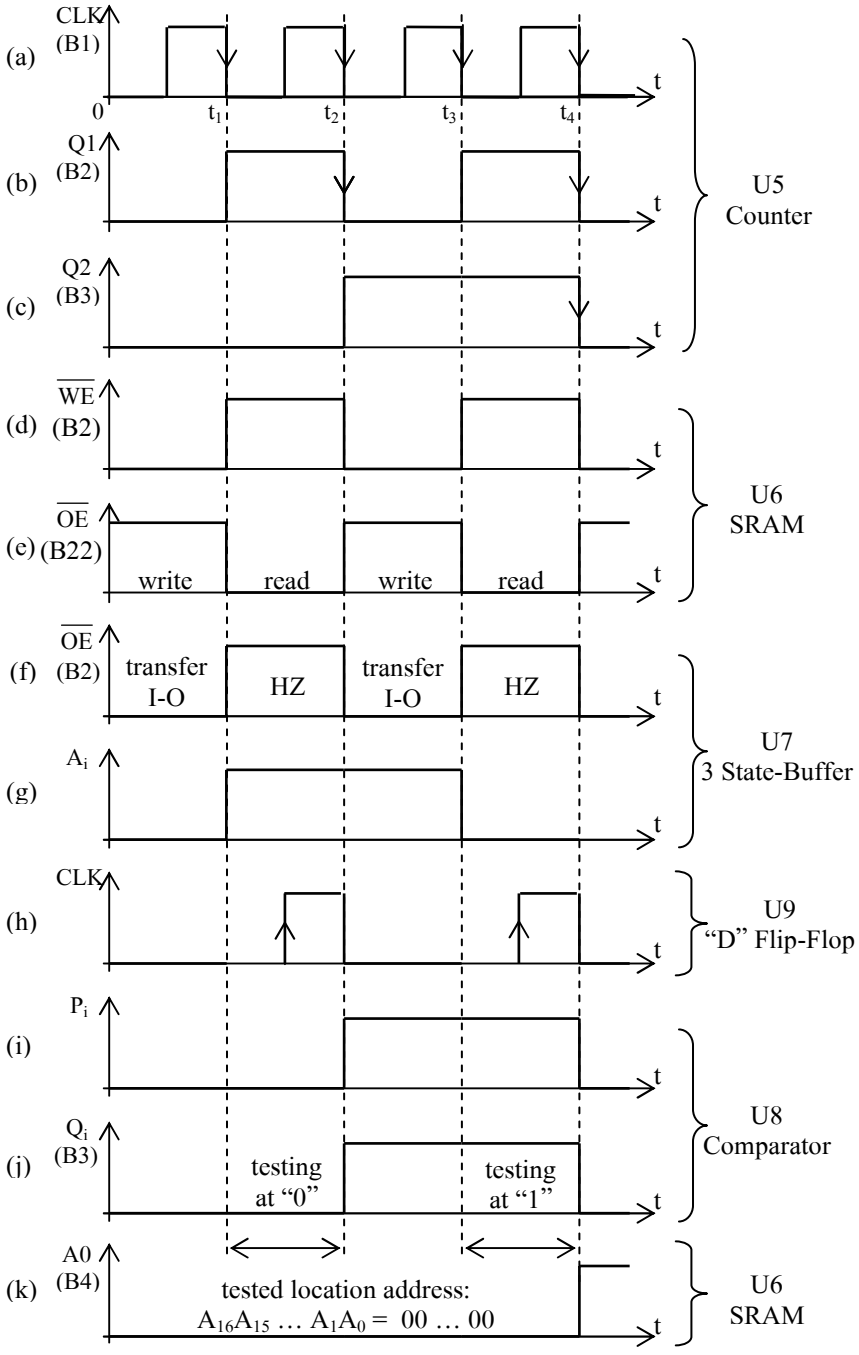

Fig. 10. The signal diagram

The 8 bits word read from memory is applied to the Pi inputs of the comparator while to its Qi inputs is applied the initial octet 00000000 (B3).

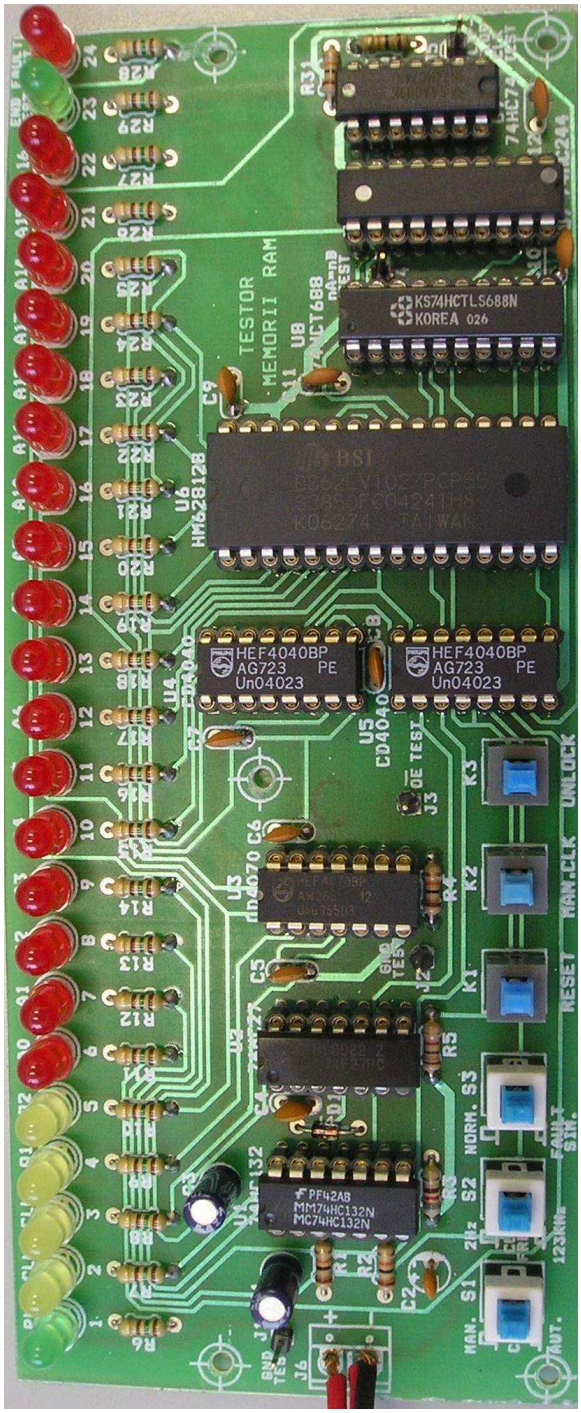

Fig. 11. The SRAM tester

If the memory does not present a fault in the 8 locations tested at 0, Pi=Qi and, to the D input of the flip-flop U9A, fig. 7, is applied 0 logic. When the increasing clock front appears, fig. 10h, at the flip-flop output is transferred 0 logic, the NOR gate U2B (fig. 2) continues to remain validated and the testing goes on.

If at least one of the 8 tested locations presents a fault of p-1 type, the comparison result will generate an 1 logic at the comparator output (B23) and, implicitly, at the D flip-flop input.
The moment the increasing clock front appears, the 1 logic is transferred at the flip-flop output, the LED 24 signalizes the fault detection, the NOR gate U2B is blocked and the testing process is stopped.

In the t_2-t_4 interval, the above described cycle is resumed and the testing at 1 logic of the same 8 memory locations takes place.

After the t_4 moment, A0 (B4)=1, the address combination becomes A16 A15 … A1 A0 = 00 …01 and the testing of a new memory octet begins. After running all the address combinations, at B21 terminal appears 1 logic, the scheme is blocked and the test is stopped.

CONCLUSIONS

The presented testing tool was much elaborated, experimentally checked and practically realized (fig. 11).
With minor modifications, it allows to test a large range of SRAM memory beginning with that standard Hitachi 8Kwords x 8bits and finishing with that 512Kwords x 8bits memory.

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