A PROGRAMMABLE ELECTRODE SUPPORT MODULE (ESM) WITH CURRENT CONVEYORS HIGH IMPEDANCE OUTPUT FOR MULTI-FREQUENCY EIT SYSTEMS

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Abstract: The paper presents a programmable current driver module for multi-frequency EIT system. The module covers two stages of the current generation: voltage to current converter and sine wave frequency and amplitude control. A original digital quadrature signal generator and a high output impedance current generator are bonded as a independent electrode module. The FPGA minimal complexity signal generator circuit as proposed is analyzed in its capacity to produce distance controllable accurate signals up 1MHz in frequency. The precision current source uses modified current conveyors of type CCII for high output impedance. Simulation results presented

Keywords: multi-frequency EIT hardware, current source, signal programmability.

1. INTRODUCTION

Electrical Impedance Tomography is yet an intensely researched domain with important recent clinical applications (Kao *et al.* 2005).

Electrical Impedance Tomography (EIT) objective is to obtain images of the internal structure of sections of the body based on tissue specific electrical property. (Borcea, 2002; Isaacson *et al.,* 2004).

The electrode module is a intense topic under investigation in prominent EIT research groups in USA and EU (Ning *et al.,* 2005; Hayatleh *et al.,* 2007).

The paper presents in part 2 a original independent programmable current driver module for multi-frequency EIT system by integrating a novel signal generator and a high output impedance source.

Part 3 of the paper present a novel sinusoidal signals generator with wide frequency range and high spectral purity based on direct digital frequency synthesis. The proposed circuit requires very few resources therefore appropriate for independent electrode module implementation (Jivet and Dragoi, 2007).

DDFS method developed in the last two decades and replaced the widely used method of analog sinusoidal signal generation based on phase looked loop (PLL) (Analog Devices, 1999; Grayver and Daneshrad, 1998). The versatility of the frequency and amplitude change are instrumental for its use in EIT multi-frequency instruments.

The performance of the proposed circuit in its capacity to generate pure and high frequency signals is presented and the FPGA efficiency of implementation.

In part 4 an original solution for the output current generator is presented. In order to obtain very high output impedance a CCII current controlled conveyor with a modified output stage solution is proposed (Minaei, *et al.,* 2002).

Simulation results indicate good output linearity and parameter in the range of the goals for the design.
Conclusions and an outline of further work are presented in part 5.

2. ELECTRODE SUPPORT MODULE (ESM)

The main objective of the ESM design was to make it independent. With a power supply and serial interface the module is intended compact to fit as near as possible the electrode.
To minimize the connecting wires to the module a serial interface assures the control link. A simple serial interface is sufficient and can be easily implemented in the same FPGA as the frequency generator module.

The signal generator as proposed requires a minimum of resources and a simple low power FPGA is a good technological first target. The DAC and filter circuits for the analog signal generation do not have critical requirements other then the 10 bit word length and similar analog accuracy and frequency of up to 1 MHz.

The current output circuit with the proposed novel design requires a custom IC.

3. DIRECT DIGITAL SYNTHESIS MODULE BASED ON AMPLITUDE SEQUENCES

A novel DDFS circuit for the generation of the sinusoidal signal was proposed that requires very few resources that will require resources found in a simple low power FPGA (Jivet and Dragoi, 2007).

The amplitude values are obtained from a extended variant of the Jordan's nonparametric circle generator algorithm. The values are the coordinates of a generic approximating point that tracks a circle following a rectangular grid according to a distance minimization criterion (Jordan, 1973)

The algorithm provides coordinate values as precise as necessary for the amplitude of sine and cosine functions.

The disadvantage of the phase compensated direct amplitude generation is a limitation in the signal maximum frequency.

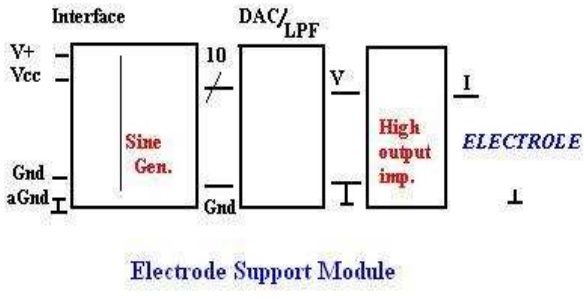

Fig. 1. A block diagram of the electrode support model for EIT system.

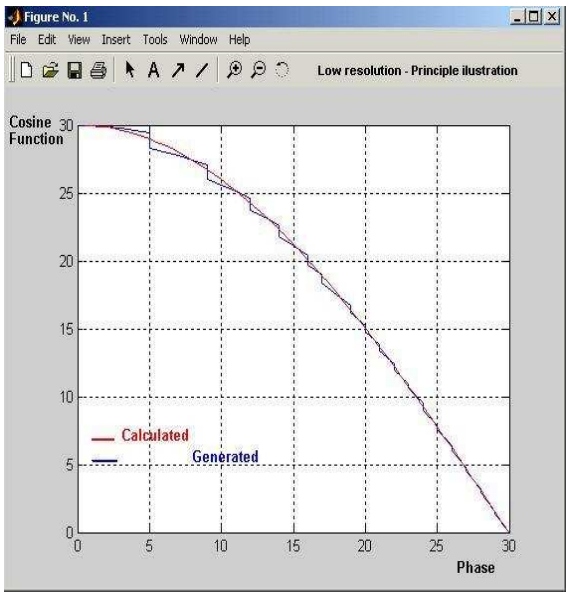

Fig. 2. Algorithmically generated digital cosine with phase compensation vs. calculated cosine.

Amplitude value sequences obtained using the proposed algorithm need to be positioned in time non uniformly requiring a minimum period in between samples to accommodate precise adjustments for minimal phase error. For the application presented in the present paper the 1 Mhz limit is attainable using any of the FPGA families in the market today.

A Matlab simulation was conducted to determine the efficiency of the proposed phase non uniformity compensation method.

The simulation showed that for 10 bit amplitude generated signal the compensation method proposed is adequate as presented in Fig. 2. It is a low resolution simulation in order to illustrate the principle.

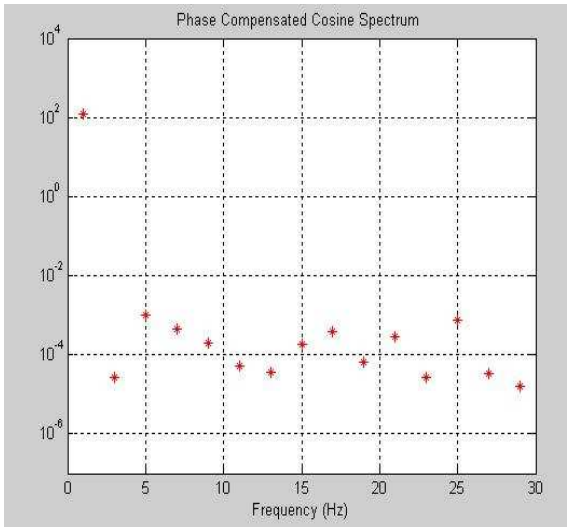

Fig. 3. Estimated power spectrum of the signal generated with the extended algorithm as proposed using phase timing compensation.

High quality signals can be generated with the extended algorithm as derived. The first harmonics which are the odd harmonics are estimated at low power levels in excess of –50 dB.

The block diagram in Fig.4 presents the principle of the proposed DDFS module. Due to the fact that the algorithm computes both the sine and cosine values a quadrature output is obtained.

The coordinate generator core implementing the algorithm in hardware receives as inputs *AT(n)* and *FT(m),* the amplitude and frequency tuning words of length *n, m*. Register *rt* and counters *ct* implement storage and general system clock *Ck* counting. The phase compensations counters *c* can be set to any resolution smaller then *n* trading accuracy to maximum signal frequency.

The module received tow inputs: a frequency tuning word and an amplitude tuning word. A solution for frequency tuning is immediate as seen in the diagram by using a period counter. The amplitude tuning is simple to implement on a cycle basis by changing the central vector length. Both the amplitude and the phase can be modified easily at the beginning of each octant hence most PSK common modulation methods are thus supported.

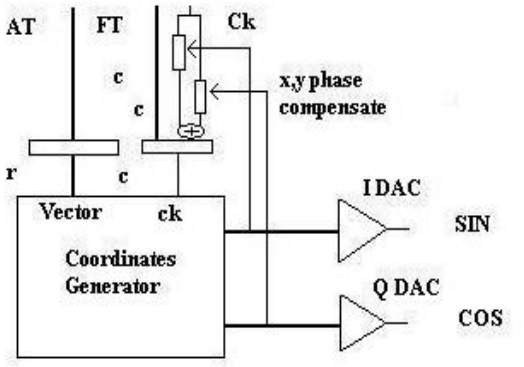

Fig. 4. Amplitude based DDFS module block diagram illustrating the principle.

Table 1 Synthesis results

DIGITSLSYNTH Project Status			
Project File:	digitslsynth.ise	Current State:	Placed and R
Module Name:	el2	• Errors:	
Target Device:	xc2v500-6fg256	• Warnings:	
Product Version:	ISE 9.1.01i	• Updated:	Mon Aug 6 2(

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	50	6,144	1%
Number of 4 input LUTs	205	6,144	3%
Logic Distribution			
Number of occupied Slices	119	3,072	3%
Number of Slices containing only related logic	119	119	100%
Number of Slices containing unrelated logic	0	119	0%
Total Number of 4 input LUTs	222	6,144	3%

Multiple discrete frequencies can be stored and loaded at the moment of generation. The control interface is the channel of communication with the control unit responsible for measurement schedule.

An implementation of the core architecture as proposed in a Xilinx FPGA was studied using a VHDL description. The VHDL structural simulation of the DDS architecture as proposed in a Xilinx ISE development environment.

The Xilinx ISE synthesis results for 16 bit version of the architecture in a Virtex II device, confirm the main advantage of the proposed architecture, one order of magnitude lower resource count compared with other DDS implementations with same resolution.

4. HIGH OUTPUT IMPEDANCE CURRENT SOURCE

An original solution for the output current generator is presented. In order to obtain very high output impedance a current controlled conveyor with a modified output stage is proposed presented in Fig. 5.

The general conditions for the voltage to current converter design where: input voltage in the frequency range up to 1Mhz and amplitude five orders of magnitude over noise and offset level, output currents of typical 1 mA on an average load impedance of 1kΩ. The central objective was an output impedance in the hundred of MΩ range.

In order to achieve the very high output impedance a CCII current controlled conveyor was modified by adding a cascode stage to the output a solution for high output impedance reported in the literature (Minaei *et al.,* 2002).

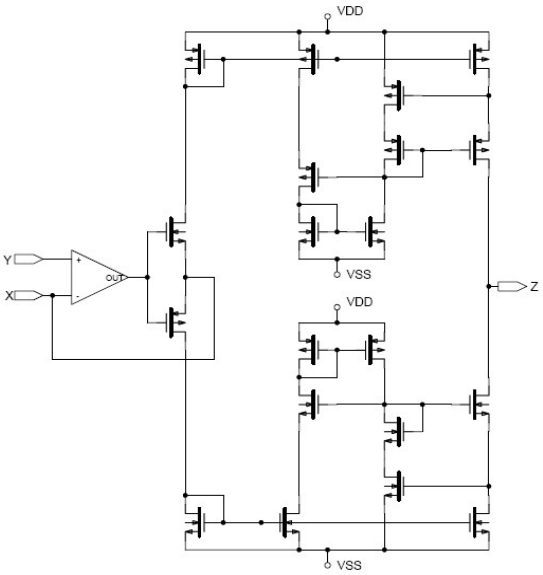

Fig. 5. Voltage to current converter with high output impedance.

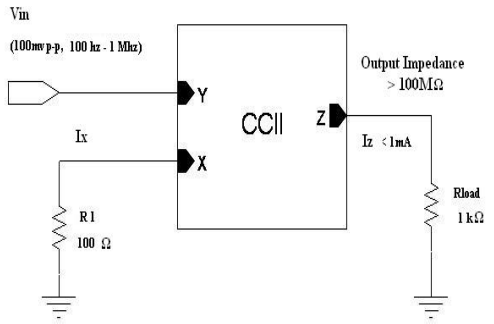

Fig. 6. Detailed schematic of current controlled conveyor CCII with high output impedance.

The detailed schematic of the conveyor is presented in Fig. 6. Simulation results show that while presenting output impedances in the hundreds of MΩ the input/output linearity is much smaller then 1% for output currents up to 1mA as can be seen in Fig. 7.

The results obtained are encouraging and further work is necessary to fine tune the part of the module to integrate with best characteristics.

5. CONCLUSIONS

A novel DDS architecture based on algorithm generated amplitude is proposed and analyzed in its capacity to produce accurate high speed sine (cosine) signals. It is also shown that most advantages of DDS architecture are preserved.

Numerical results of the simulations indicate that using the proposed architecture in nowadays FPGA's or ASIC implementation one can generate low harmonic signals up to frequencies in the MHz range. The resources necessary in FPGA implementation for 16 bit resolution is less then 100 slices/cells factor of 10 below other architectures in use today.

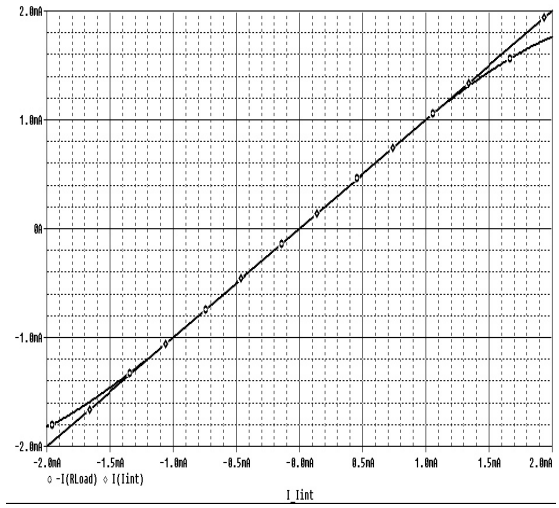

Fig. 7. X input /Z output currents linearity simulation.

The current controlled current source CCII with cascode output proves a promising solution for very high output impedance and good linearity.

Further work is necessary to fine tune and match the characteristics of the two main parts of the electrode support module.

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