Abstract: This paper presents a current mode (translinear) technique for low voltage, continuous-time, analogue filter implementation. Firstly, the state-space description of current-mode filter is presented. Then the current-mode integrator based on translinear approach is presented and analyzed. Finally, as a test vehicle for the proposed technique, a low voltage, third order, continuous-time filter, for low power applications structure implementation is described.

Keywords: Analogue signal processing circuits, translinear circuits, CMOS analogue filters, low power and low voltage circuits.

1. INTRODUCTION

The existing CMOS technologies provide ample opportunity to integrate entire system on a single chip. To date, the ability to integrate large digital systems has far out weighted the ability to integrate the analogue systems. The greatest impediment to analogue CMOS VLSI design has been the difficulty to get consistent circuit performance over the broad range of requirements for signal gain, frequency and/or phase response, delay, power consumption and signal integrity. In the same time the analogue design in mixed signal environments becomes more difficult and challenging as the IC’s power supply voltage scales down, to the values slightly higher than the MOS threshold voltage.

The translinear circuits, due to their current domain operation, are suitable for low supply voltage operation. In translinear circuits the MOS transistors usually operate in weak inversion (or sub-threshold) region, (Enz et al., 1995), where the current-voltage characteristic is exponential. The main problems associated to the sub-threshold region operation are the relatively low speed capability and inferior matching. But these problems are relatively solved in sub-micron technology.

This paper presents a synthesis technique for continuous time current-mode filters operating at very low supply voltage. The basic current-mode integrator is analyzed and finally the structure of a third order current-mode filter is presented. This technique can be extended, (Doicaru, 2007), in order to optimize performances like bandwidth, noise, errors due to mismatching and dynamic range.

2. THE STATE-SPACE DESCRIPTION AND SYNTHESIS OF CURRENT-MODE FILTER

This section presents the way the intermediate transfer function synthesis method (Snelgrove et al., 1986) can be used in current-mode domain filters. The method was developed for AO-RC filter; basically a given n-th order transfer function is realized using n resistively interconnected integrators. The design process comprises two steps: firstly a set of intermediate transfer functions (IFs) is selected and then the set is using in synthesis of circuit that realized the given transfer function. The major advantage of this method is that the filter’s performance evaluation and optimization can be performed at the abstract level of transfer function generation and not at the circuit topology level.
The state-variable formulation of the AO-RC is:

\[ s \cdot x(s) = A \cdot x(s) + b \cdot u(s) + e(s) \]

\[ y(s) = c^T \cdot x(s) + d \cdot u(s) \]  

where the vector \( x(s) \) represents the circuit state (integrators outputs), matrix \( A \) describes the interconnections between the \( n \) integrators, vector \( b \) contains the coefficients that multiply the input signal \( u(s) \) in order to be applied to the integrators inputs, vector \( c \) contains the coefficients required to form the output, scalar \( d \) is the coefficient of the feedthrough component from input to output, and \( e(s) \) is the vector containing the noise at the integrator inputs.

The dual sets of IFs, \( \{f(s)\} \) and \( \{g(s)\} \) are given by:

\[ f_i(s) = \frac{x_i(s)}{u(s)}; \quad f(s) = (s - I - A)^{-1} \cdot b \]

\[ g_i(s) = \frac{y(s)}{y_i(s)}; \quad g^T(s) = c^T \cdot (s - I - A)^{-1} \]  

The set \( \{f(s)\} \) contains the transfer function from the filter input to the integrator outputs, and the set, \( \{g(s)\} \), can be physically interpreted as the integrators noise gains. Given a transfer function \( t(s) \), IF synthesis is based on choosing a set of linearly independent functions, \( \{f(s)\} \), having identical denominator polynomials, \( e(s) \), and arbitrary numerator polynomials of degree less than \( n \). From this set the \( \{A, b, c, d\} \) parameters can be obtained using the following relation:

\[ A = F \cdot E \cdot F^{-1}, \quad b = F \cdot 1, \quad c^T = t^T \cdot F^{-1}, \]

\[ d = t_n+1, \quad t(s) = t^T \cdot v(s) + t_{n+1}, \]

\[ f(s) = F \cdot v(s), \quad g(s) = G \cdot v(s), \]

\[ v_i(s) = \frac{1}{s}, \quad i = 1, n, \]

\[ G^T = H \cdot F^{-1} \]  

where \( t \) is a vector containing the \( t(s) \) \( n \) residues at the poles, \( t_{n+1} \) – the residue at \( s=\infty \), \( F \) – a matrix containing the residues of the \( f \) functions evaluated at the poles, \( G \) – a matrix of the residues of the \( g \) functions, \( e_i \) – the \( e(s) \) roots, \( E \) – the diagonal matrix having the natural modes \( e_i \) as its elements, \( H \) – a diagonal matrix formed from the residues of \( t(s) \), and \( I = (1, 1, \ldots, 1)^T \).

The sensitivities of filter directly depend of IFs set:

\[ S_{b_i}^{(s)} = g_i(s) \cdot f_i(s) \cdot \frac{A_{b_j}}{t(s)} \]

\[ S_{b_i}^{(s)} = g_i(s) \cdot \frac{b_j}{t(s)} \cdot S_{f_i}^{(s)} = f_i(s) \cdot \frac{e_i}{t(s)} \]

\[ S_{d}^{(s)} = \frac{d}{t(s)} \cdot S_{f_i}^{(s)} = f_i(s) \cdot \frac{s}{t(s)} \]

\[ S_{\mu_i}^{(s)} = S_{b_i}^{(s)} \cdot S_{f_i}^{(s)} \]

In the above equations \( g_i \) is the integrator gain and \( \mu_i \) is the operational amplifier gain.

Noise signals injected at integrator inputs can be modelled by \( e(s) \). Assuming white input noise, with spectral density \( N_i^2 \), the output noise power spectrum is given by:

\[ P_n(\omega) = N_i^2 \cdot \sum_{i} |g_i(j\omega)|^2 \]

with a rms level of:

\[ \|P_n(\omega)\| = N_i^2 \cdot \sqrt{\sum_{i} |g_i(j\omega)|^2} \]

This description can be adapted to the current-mode filter. The current through the \( k \)-th capacitor of the current-mode filter is:

\[ C_k \nu_{C_k} = i_{C_k} + i_{C_k} + \ldots + i_{C_{kn}} + i_{C_{bk}} = \]

\[ = a_{k1}i_1 + a_{k2}i_2 + \ldots + a_{kn}v_n + b_{k}i_{in} + \epsilon_k \]

where \( i_{C_k}, k, j=1+n \), is the \( k \)-th capacitor current component dependent on output current \( i_j, j=1+n \), \( i_j \) is the \( j \)-th current-mode integrator output current, \( i_{in} \) is the input current, \( a_{kj}, k=1+n \), \( b_k \), \( k=1+n \), coefficients describes the capacitor current components dependence on the output currents of the current-mode integrators, respectively, on the filter input current, and \( \epsilon_k = \sum_j \epsilon_{kj} \) is the total noise current through capacitor.

Using convenient circuit technique to implement a logarithmic dependence between capacitor voltage, \( \nu_{C_k} \), and output current of current-mode integrator, \( i_{is} \),

\[ \nu_{C_k} = V_c \ln \left( \frac{i_{is}}{I_c} \right) \]

where \( V_c \) and \( I_c \) are scale factors, the capacitor voltage derivative, \( \nu_{C_k} \), becomes:

\[ \frac{d \nu_{C_k}}{dt} = \frac{V_c}{i_{is}} \frac{di_{is}}{dt} \]

Using the translinear loops one get for each component of the capacitor current:

\[ i_{C_k} - i_{k} = a_{kj}i_j \cdot \nu_{C_k} = \frac{\epsilon_k}{b_k} \rightarrow \epsilon_k = \frac{b_k}{(C_k \nu_{C_k})} \]

and equation (8) becomes:

\[ \frac{di_{is}}{dt} = a_{k1}i_1 + a_{k2}i_2 + \ldots + a_{kn}v_n + b_k i_{in} + \epsilon_k \]

where:

\[ a_{kn} = a_{kn} / (C_k \nu_{C_k}), b_k = b_k / (C_k \nu_{C_k}), \epsilon_k = \frac{\epsilon_k}{(C_k \nu_{C_k})} \]

The circuit resulted by interconnection of \( n \) current mode integrators with translinear loops can be described by the same state-variable formulation (1):

\[ s \cdot x(s) = A \cdot x(s) + b \cdot i_{in}(s) + e(s) \]

\[ i_{out}(s) = c^T \cdot x(s) + d \cdot i_{in}(s) \]

where the states \( x_i \) are represented by the integrators output current, matrix element \( A_{ij} \) is implemented by a translinear loop with input current \( x_i \) and output the component \( i_{C_k} \) of the current through \( k \)-th, the vector
element $b_k$ is implemented by translinear loop from the input $i_{k_0}$ to state $k$, $c_k$ is multiplication coefficient of state $k$ required to form the output current of the filter $i_{k_0}$. $d$ is multiplication coefficient of input current $i_{k_0}$ and $e(s)$ can model the current noise at the input of the $k$-th current integrator.

So the meaning of $\{g_k(s)\}$ IF's set is the same as in the OA-RC filter synthesis (the state $k$ and the input signal ratio) and the physical meaning of $\{g_k(s)\}$ IF's set is the noise gain to the input of integrator $k$ at output of filter. We can conclude that the all results obtained in the OA-RC filter synthesis can be applied to the current-mode filter synthesis.

3. MOS TRANSISTOR CURRENT-VOLTAGE CHARACTERISTICS

This section presents a brief review of the MOS transistor I-V characteristics, focused on weak inversion operation.

The MOS transistor drain current equation valid in all operating regions is (Enz et al., 1995):

$$ I_D = \beta \int_{V_S}^{V_{DS}} (-Q_i/C_{ox}) \, dV \quad (15) $$

with

$$ \beta = \mu C_{ox} (W/L) \quad (16) $$

where $W$ and $L$ are the channel width and length, $C_{ox}$ = gate capacitance per unit area, $\mu$ = charge carrier mobility, $Q_i$ = induced mobile charge in channel, $V_{DS}$ = drain, source voltages referred to the local substrate, $V$ = channel potential. Equation (15) may be decomposed, (Vittoz, 1994), into:

$$ I_D = \beta \int_{V_S}^{V_{DS}} (-Q_i/C_{ox}) \, dV - \beta \int_{V_T}^{V_{GS}} (-Q_i/C_{ox}) \, dV $$

$$ = I_F - I_R \quad (17) $$

where $I_F$ is called forward current (controlled by source voltage $V_S$) and $I_R$ is called reverse current (controlled by drain voltage $V_D$). Taking into account weak inversion channel charge dependency on channel potential

$$ Q_i/C_{ox} \sim e^{(V_{p-V})/V_T} \quad (18) $$

$I_F$ and $I_R$ are given by

$$ I_{F(R)} \sim \beta e^{(V_{p-V_{SD,1}})/V_T} \quad (19) $$

And the drain current equation results:

$$ I_D = I_S e^{V_p/V_T} \left[ e^{-V_S/V_T} - e^{-V_D/V_T} \right] \quad (20) $$

In terms of $V_{GS}$ and $V_{GD}$ equation (20) becomes

$$ I_D = I_S e^{(V_p-V_{G})/V_T} \left[ e^{-V_{GS}/V_T} - e^{-V_{GD}/V_T} \right] \quad (21) $$

where $I_S$ is a specific current (limit of weak inversion), proportional to $W/L$.

$$ I_S e^{(V_p-V_{G})/V_T} = \frac{W}{L} I_0(V_G) \quad (22) $$

$I_0(V_G)$ is the square transistor zero-bias ($V_{GS} = 0$) current.

Using (22) $I_F$ and $I_R$ equations become:

$$ I_F = \frac{W}{L} I_0(V_G) \cdot e^{V_{GS}/V_T} \quad (23) $$

$$ I_R = \frac{W}{L} I_0(V_G) \cdot e^{V_{GD}/V_T} $$

If $I_R < I_F$, the MOS transistor is saturated, otherwise is non-saturated.

In Fig. 1.a are shown the two operation regions for weak inversion case, that are defined by the ratios $I_D/I_F$ and $V_{DS}/V_T$.

Therefore, each of the drain current components, equation (22), of a non-saturated transistor may be relate to an equivalent saturated transistor with voltages $V_{GS}$ and $V_{GD}$. The non-saturated transistor may be decomposed into two identical saturated transistors anti-parallel connected, (Vittoz and Fellrath, 1997), see Fig. 1.b. The dashed line transistor corresponds to the reverse current component, and represents the effect of the non-saturated operation of the real transistor.

4. THE BASIC CURRENT-MODE INTEGRATOR

This section presents the intermediate transfer function synthesis method (Snelgrove et al., 1986) in current-mode domain.

The basic current-mode integrator schematic, with its translinear loop for an $i_{C_0}$, is presented in Fig. 2a. and its symbolic representation in Fig. 2.b. The minimum supply voltage required for this circuit is given by the MOS transistor threshold voltage plus the drain-source saturation voltage. Due to this low voltage value the transistors $M_4$, $M_{13}$, $M_2$ and $M_6$ are non-saturated.
Applying the Kirchhoff law to these translinear loops transistors $M_3$, Fig. 2.b) were added in order to account the non-saturated operation of these transistors. This way all transistors can now be regarded as saturated, $I_p < I_r$, and to a good approximation

$$I_{Di} = I_{Fi} = (W_i / L_i) \cdot I_0(V_G) \cdot e^{V_{GS}/V_T} \quad i = 1, 10$$

(24)

The integrator has four local loops: (1) $M_1$, $M_5$, $M_{4*}$, $M_3$, (2) $M_1$, $M_5$, $M_{6*}$, $M_7$; (3) $M_1$, $M_{2*}$, $M_4$, $M_T$, (4) $M_{14}$, $M_{13*}$, $M_{16}$, $M_{15}$; and a general translinear loop (5) $M_1$, $M_5$, $M_{10}$, $M_8$, $M_T$, $M_8$.

Applying the Kirchhoff law to these translinear loops one gets:

$$V_{G51} - V_{G55} = V_{G53} - V_{G54*}$$
$$V_{G51} - V_{G55} = V_{G57} - V_{G56*}$$
$$V_{G514} - V_{G512*} = V_{G515} - V_{G516}$$
$$V_{G51} - V_{G55} + V_{G510} = V_{G59} - V_{G58} + V_{G57}$$

(25)

Using equations (24) and assuming the equal-sized transistors the translinear loops equations become:

$$\begin{align*}
V_T \ln \frac{I_{D1}}{I_0(V_{G1})} - V_T \ln \frac{I_{D5}}{I_0(V_{G5})} &= \quad (1) \\
V_T \ln \frac{I_{D1}}{I_0(V_{G1})} - V_T \ln \frac{I_{D5*}}{I_0(V_{G5})} &= \quad (2) \\
V_T \ln \frac{I_{D5}}{I_0(V_{G5})} - V_T \ln \frac{I_{D5*}}{I_0(V_{G5})} &= \quad (3) \\
V_T \ln \frac{I_{D1}}{I_0(V_{G1})} - V_T \ln \frac{I_{D4*}}{I_0(V_{G4})} &= \quad (4) \\
V_T \ln \frac{I_{D5}}{I_0(V_{G5})} - V_T \ln \frac{I_{D5*}}{I_0(V_{G5})} &= \quad (5)
\end{align*}$$

(26)

From (25) and assuming that $I_0(V_{G1}) = I_0(V_{G5})$, the equations (26)-(29) become:

$$\begin{align*}
V_T \ln \frac{I_{D1}}{I_0(V_{G1})} - V_T \ln \frac{I_{D5}}{I_0(V_{G5})} &= \quad (26) \\
V_T \ln \frac{I_{D1}}{I_0(V_{G1})} - V_T \ln \frac{I_{D5*}}{I_0(V_{G5})} &= \quad (27) \\
V_T \ln \frac{I_{D5}}{I_0(V_{G5})} - V_T \ln \frac{I_{D5*}}{I_0(V_{G5})} &= \quad (28)
\end{align*}$$

(29)

It can be seen that the oppositely connected transistor pairs have the same gate voltage. Also, have the same gate voltage the following transistor pairs $M_2$-$M_{4*}$, $M_1$-$M_5$, $M_{2*}$-$M_4$, $M_{14}$-$M_{13*}$, $M_{16}$-$M_{15}$, $M_{10}$-$M_8$. It follows that

$$\begin{align*}
I_0(V_{G1}) &= I_0(V_{G2}) = I_0(V_{G2*}) = I_0(V_{G3}) \\
I_0(V_{G7}) &= I_0(V_{G8}) = I_0(V_{G8*}) = I_0(V_{G9}) \\
I_0(V_{G14}) &= I_0(V_{G13}) = I_0(V_{G13*}) \\
I_0(V_{G15}) &= I_0(V_{G16}) = I_0(V_{G16*}) \\
I_0(V_{G9}) &= I_0(V_{G10})
\end{align*}$$

(30)

and the equations (26)-(29) become the classical translinear relation independent of the body effect:

$$\begin{align*}
\frac{I_{D1}}{I_0(V_{G1})} &= \frac{I_{D3}}{I_0(V_{G3})} = \frac{I_{D5}}{I_0(V_{G5})} = \frac{I_{D6}}{I_0(V_{G6})} = \frac{I_{D4*}}{I_0(V_{G4})} = \frac{I_{D5*}}{I_0(V_{G5})} = \frac{I_{D6*}}{I_0(V_{G6})} = \frac{I_{D4}}{I_0(V_{G4})} = \frac{I_{D5}}{I_0(V_{G5})} = \frac{I_{D6}}{I_0(V_{G6})} \\
\frac{I_{D1}}{I_0(V_{G1})} &= \frac{I_{D7}}{I_0(V_{G7})} = \frac{I_{D6}}{I_0(V_{G6})} = \frac{I_{D5}}{I_0(V_{G5})} = \frac{I_{D4*}}{I_0(V_{G4})} = \frac{I_{D5*}}{I_0(V_{G5})} = \frac{I_{D6*}}{I_0(V_{G6})} = \frac{I_{D4}}{I_0(V_{G4})} = \frac{I_{D5}}{I_0(V_{G5})} = \frac{I_{D6}}{I_0(V_{G6})}
\end{align*}$$

(31)

(32)

Substituting into (32) the corresponding drain currents results:
\[ I_{D4^*} = \frac{(i_{in} + I_{IN}) I_0}{I_0 + I} \]
\[ I_{D6^*} = \frac{(i_{out} + I_{OUT}) I_0}{I_0 + I} \]
\[ I_{D2^*} = \frac{(I_0 + I) I_0}{i_{out} + I_{OUT}} \]
\[ I_{D13^*} = \frac{I I_{IN}}{i_{out} + I_{OUT}} \]
\[ I_0 + I = \frac{I_{D10} = I_{D4^*} - I_{D5^*} + I_{D6^*} - I_{D6^*}}{I_0 + I} \]
\[ i_{out} + I_{OUT} = \frac{(i_{in} + I_{IN}) I_0 - I_0 + I_{OUT}}{I_0 + I} \]
\[ (i_{in} + I_{IN}) I = \frac{(i_{in} + I_{IN}) I_0}{I_0 + I} \]
\[ (I_{IN}) - (I_{IN}) - (I_{IN}) = \frac{(I - I_{IN}) - (I_{IN}) - (I_{IN})}{i_{out} + I_{OUT}} \]

Substituting equations (33) and (34) into general translinear loop equations (32) yields:
\[ (i_{in} + I_{IN}) I = (i_{in} + I_{IN}) (i_{out} + I_{OUT}) \]
\[ (i_{in} + I_{IN}) I = i_{C} (i_{out} + I_{OUT}) + I I_{IN} \]
\[ i_{in} I = i_{C} (i_{out} + I_{OUT}) \]
\[ i_{C} = C \frac{d v_{C}}{dt} \]
\[ i_{C} = \frac{C V_T}{i_{out} + I_{OUT}} \frac{di_{out}}{dt} \]

Finally we get a linear integrator function:
\[ i_{out} = \frac{I}{C V_T} \int i_{in} dt \]

The integrator operates correctly as long as the quiescent values of the currents \( I, I_{in}, I_{IN}, I_{OUT} \) is chosen so that the integrator’s transistors drain currents to be strictly positive for the input voltage range, (Seevinck, 1988).

5. THE THIRD ORDER CURRENT MODE FILTER

As an example of the application of the synthesis technique presented in Section 2 a third order current mode filter have been synthesised. The transfer function of the filter is:
\[ t(s) = \frac{1}{s^3 + 2s^2 + 2s + 1} \]

The system parameters \( \{A,b,c,d\} \) resulted using the SSAF program (Doicaru et. al., 2007) for orthonormal IFs are:
\[ A = \begin{bmatrix} 0 & 0.707 & 0 \\ 0 & -1.225 & -2 \\ -0.707 & 0 & 1.225 \end{bmatrix} \]

\[ b = \begin{bmatrix} 0 \\ 0 \\ 0.798 \end{bmatrix} \]

\[ c = \begin{bmatrix} 0 \\ 0 \\ 1.447 \end{bmatrix} \]

\[ d = 0 \]

We choose this type of IFs to be generated by SSAF because the structures to be synthesised using orthonormal intermediate transfer functions generally have good dynamic range, good signal swing and low sensitivity.

The structure of the current mode filter characterised by parameters (42) is presented in Fig. 3 and the system equation are:
\[ i_{C1} = i_{C12} \]
\[ i_{C2} = i_{C22} + i_{C23} \]
\[ i_{C3} = i_{C31} + i_{C32} + i_{C33} \]
\[ i_{out} = c_3 i_{out3} \]
Using the relations developed in Section 3 the system (43) becomes:

\[
\frac{C_1 V_T}{i_{out1} + I_{OUT1}} \frac{d}{dt} i_{out1} = i_{out2} + I_{12}.
\]

\[
\frac{C_2 V_T}{i_{out2} + I_{OUT2}} \frac{d}{dt} i_{out2} = \frac{i_{out3} + I_{22}}{i_{out3} + I_{OUT3}}
\]

\[
\frac{C_3 V_T}{i_{out3} + I_{OUT3}} \frac{d}{dt} i_{out3} = \frac{i_{out1} + I_{32}}{i_{out1} + I_{OUT1}}
\]

(44)

and the state-space description of this filter is:

\[
\frac{d}{dt} i_{out1} = \frac{i_{out2} + I_{12}}{C_1 V_T}.
\]

\[
\frac{d}{dt} i_{out2} = \frac{i_{out3} + I_{22}}{C_2 V_T} - \frac{i_{out1} + I_{32}}{C_2 V_T}.
\]

\[
\frac{d}{dt} i_{out3} = \frac{i_{out1} + I_{32}}{C_3 V_T} + \frac{i_{out2} + I_{22}}{C_3 V_T}.
\]

(45)

It is obvious that:

\[
a_{12} = \frac{I_{12}}{C_1 V_T};
\]

\[
a_{22} = \frac{I_{22}}{C_2 V_T};
\]

\[
a_{31} = \frac{I_{31}}{C_3 V_T};
\]

\[
a_{32} = \frac{I_{32}}{C_3 V_T};
\]

\[
b_3 = \frac{I_{b3}}{C_3 V_T};
\]

\[
c_3 = \frac{(W/L)_{\text{nMOS}}}{(W/L)_{\text{IDL3}}}.
\]

(46)

In the future work the current-mode filters synthesis method presented in this paper will be refined being focused on optimization of specific performances like bandwidth, noise, errors due mismatching and dynamic range.

6. CONCLUSIONS

Future analogue circuits will have to operate successfully at supply voltages slightly higher than the MOS transistor threshold voltage. So, the suitable topologies for signal processing at such low values of supply voltages are the translinear circuits because they are operating in current domain and in this way the very small voltage swings are avoided.

This paper presented a technique for very low supply voltage, continuous time, current-mode filters synthesis based on the intermediate transfer functions method. This method has the distinct advantage of filter performance optimization at the abstract level of IFs, not at the topological level. In paper is also presented the basic cell of the filter – the current mode integrator, suitable for static and dynamic analogue signal processing and very low supply voltage operation. The minimum value of supply voltage required for this circuit is given by the sum of the MOS transistor threshold voltage and the drain-source saturation voltage.

All transistors of these networks operate in weak inversion due to the requirements of translinear principle to have an exponential I-V characteristic and the very low power supply voltage. Therefore, bandwidth will be limited and the circuits will be sensitive to the threshold voltage matching. Finally, as a test vehicle for the proposed synthesis method, the structure of a third order continuous-time filter for low power applications was presented and analyzed.

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