A FULLY DIFFERENTIAL SWITCHED CAPACITOR AMPLIFIER MODELLING AND PARAMETER EVALUATION

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Abstract: This paper develops an analytical model for a standard topology, fully differential, switched capacitor amplifier; including the base amplifier offset voltage and common mode range, and capacitor mismatch effects. The amplifier is designed in a 0.6 µm process and the analytical model accuracy is compared with the simulation results.

Keywords: switched capacitor amplifier, fully differential

1. INTRODUCTION

The design of CMOS precision circuits is challenged by poor transistor matching. The switched capacitor (SC) approach is a natural one, taking into account the availability of switches and capacitors in the CMOS processes. The SC technique provides low offset voltages, due to offset compensation (correlated double sampling technique) and high gain accuracy, due to good capacitor matching. (Enz, 1996)

In a sample data system, the discrete time involved by a SC topology is not a drawback and the high frequency clock is already part of the system. A classical example is the analog to digital converter. Also, the SC approach can be used for "continuous time" circuits, by filtering the output.

2. FULLY DIFFERENTIAL SC AMPLIFIER

In this paper, a fully differential single stage switched capacitor amplifier is implemented and analyzed. The basic schematic is presented in Fig. 1 (Schoenberg, 1991). For the base amplifier, folded cascade topology was preferred, as it provides the high frequency performances needed at reasonable area consumption and gain. For a fully differential amplifier, a common mode feedback stage is needed to control the amplifier's output common mode.

Two non overlapping clock signals are used to control the switches. The circuit functioning has two phases: the "input sampling" phase, when input voltage are sampled on C_{11}, C_{12} capacitors and the "signal evaluation" phase, when the output voltage is developed, by transferring the charge from C_{11} to C_{21} and respectively from C_{12} to C_{22}. The common mode feedback block and the non overlapping clock generator implementation is not discussed in this paper.

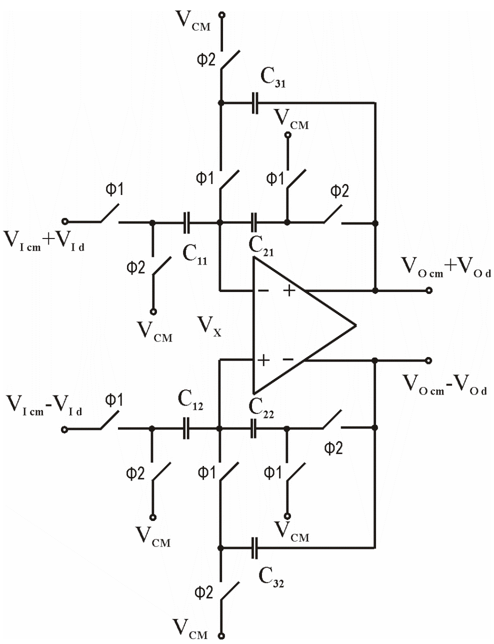

Fig. 1. Fully differential SC Amplifier topology.

3. SC AMPLIFIER ANALYSIS

In this section, we analyze the behavior and develop an analytical model for the SC amplifier presented in Fig. 1. There are many methods, present in literature, of analyzing a SC circuit. We shall adopt a direct method of evaluating the charge stored on each capacitor during each phase, and then apply the charge conservation principle at phase transitions.

3.1 Input Sampling Phase

The circuit configuration corresponding to the *input sampling* phase is presented in Fig. 2. (The Φ_1 phase switches are *on* and Φ_2 phase switches are *off*.) At the input, we apply a common mode voltage, V_{Icm} and a differential voltage, V_{Id}, both signals are lower frequency signals and can be consider constant during a clock cycle. The amplifier output voltage also consists of a common mode component, V_{Ocm}, controlled by the common mode feedback block and the differential component, V_{Od}.

To model the offset voltage, we consider V_x to be the middle base amplifier input voltage. From V_x, we shift the negative input with +Vos/2 and the positive one with −Vos/2 (see Fig. 2). An internal common mode voltage, V_{CM}, is used as a "common point" for capacitor charging. The charges stored on each capacitor during the *input sampling* phase, Φ_1, are given by: (Martin, 1987)

$$Q_{11}(\Phi_1) = C_{11}\left(V_{Icm} + V_{Id} - V_X(\Phi_1) - V_{os}/2\right) \quad (1)$$

$$Q_{21}(\Phi_1) = C_{21}\left(V_X(\Phi_1) + V_{os}/2 - V_{CM}\right) \quad (2)$$

$$Q_{31}(\Phi_1) = C_{31}\left(V_{Ocm} + V_{Od}(\Phi_1) - V_X(\Phi_1) - V_{os}/2\right) \quad (3)$$

and respectively

$$Q_{12}(\Phi_1) = C_{12}\left(V_{Icm} - V_{Id} - V_X(\Phi_1) + V_{os}/2\right) \quad (4)$$

$$Q_{22}(\Phi_1) = C_{22}\left(V_X(\Phi_1) - V_{os}/2 - V_{CM}\right) \quad (5)$$

$$Q_{32}(\Phi_1) = C_{32}\left(V_{Ocm} - V_{Od}(\Phi_1) - V_X(\Phi_1) + V_{os}/2\right) \quad (6)$$

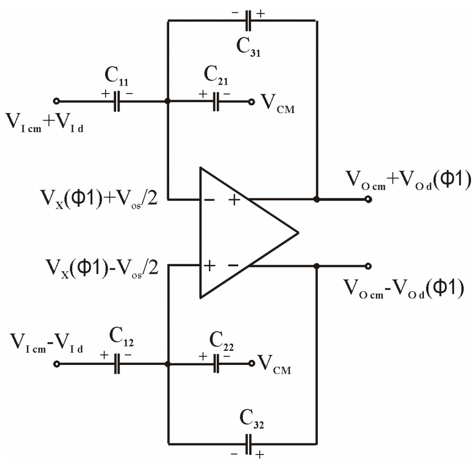

Fig. 2. SC Amplifier configuration in input sampling phase.

3.2 Signal Evaluation Phase

The circuit configuration corresponding to the signal evaluation phase is presented in Fig. 3. (The Φ_1 phase switches are *off* and Φ_2 phase switches are *on*.)

The output differential voltage, V_{Od}, and the base amplifier input voltage, V_x, have changed during the phase transition. This change is denoted by using the Φ_2 index. The new capacitor charges are given by:

$$Q_{11}(\Phi_2) = C_{11}\left(V_{CM} - V_X(\Phi_2) - V_{os}/2\right) \quad (7)$$

$$Q_{21}(\Phi_2) = C_{21}\left(V_X(\Phi_2) + V_{os}/2 - V_{Ocm} - V_{Od}(\Phi_2)\right) \quad (8)$$

$$Q_{31}(\Phi_2) = C_{31}\left(V_{Ocm} + V_{Od}(\Phi_2) - V_{CM}\right) \quad (9)$$

and respectively

$$Q_{12}(\Phi_2) = C_{12}\left(V_{CM} - V_X(\Phi_2) + V_{os}/2\right) \quad (10)$$

$$Q_{22}(\Phi_2) = C_{22}\left(V_X(\Phi_2) - V_{os}/2 - V_{Ocm} + V_{Od}(\Phi_2)\right) \quad (11)$$

$$Q_{32}(\Phi_2) = C_{32}\left(V_{Ocm} - V_{Od}(\Phi_2) - V_{CM}\right) \quad (12)$$

All capacitor charges were considered with the sign indicated in Fig. 2 and respectively Fig. 3.

3.3 Phase transfer

In both phases, the A and B nodes are connected only to the base amplifier inputs and to capacitors. Assuming that no current is flowing through the base amplifier input, the charge conservation principle requires that the charge is only moved from one capacitor to the other, but the total charge is constant. We shall use the ΔQ_{ij} notation for the charge variation on C_{ij} capacitor during a phase transition

$$\Delta Q_{ij} = Q_{ij}(\Phi_1) - Q_{ij}(\Phi_2) \quad (13)$$

After the $\Phi_1 \rightarrow \Phi_2$ transition, node A is only connected to C_{11} and C_{21} capacitors and the base amplifier's input. The total charge stored on C_{11} and C_{21} remains constant, $\Delta Q_{11}=\Delta Q_{21}$. Similar considerations in node B lead to $\Delta Q_{12}=\Delta Q_{22}$.

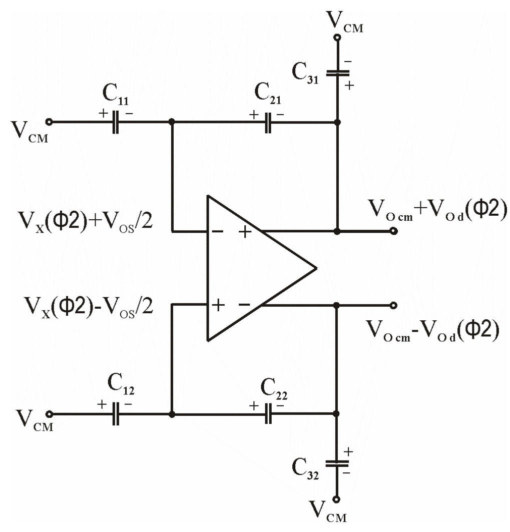

Fig. 3. SC Amplifier configuration in output evaluation phase.

After $\Phi_2 \rightarrow \Phi_1$ transition, node A is connected to C_{11}, C_{21} and C_{31} capacitors (and the base amplifier's input). The total charge stored on all capacitors must remain constant. We know from the $\Phi_1 \rightarrow \Phi_2$ transition that $\Delta Q_{11}=\Delta Q_{21}$ so it results that the charge on C_{31} capacitor is also constant $\Delta Q_{31}=0$. Similarly, we deduce that $\Delta Q_{32}=0$. The equations describing the phase result:

$$\Delta Q_{11} = \Delta Q_{21} \qquad \Delta Q_{12} = \Delta Q_{22} \tag{14}$$

$$\Delta Q_{31} = 0 \qquad \Delta Q_{32} = 0 \tag{15}$$

Or, explicitly:

$$Q_{11}(\Phi_1) - Q_{11}(\Phi_2) = Q_{21}(\Phi_1) - Q_{21}(\Phi_2) \tag{16}$$

$$Q_{12}(\Phi_1) - Q_{12}(\Phi_2) = Q_{22}(\Phi_1) - Q_{22}(\Phi_2) \tag{17}$$

$$Q_{31}(\Phi_1) - Q_{31}(\Phi_2) = 0 \tag{18}$$

$$Q_{32}(\Phi_1) - Q_{32}(\Phi_2) = 0 \tag{19}$$

These four equations, together with capacitor charge equations, (1) – (12), completely describe the two system phases.

4. OUTPUT VOLTAGE MODEL

Our main target is to develop a model for the output voltage, in both operation phases, taking into account the offset voltage and capacitor mismatch effects. To this end, we shall solve this previous system in respect to the output differential voltage and the base amplifier input voltage.

As it will be showed in Section 5.3, modeling the base amplifier input voltage, V_x, is also very important as it has direct influence on the SC Amplifier input common mode voltage range.

To simplify the presentation, we shall first present the ideal case and develop the basic model for this stage. Then we shall consider the offset voltage and capacitor mismatch effects, and determine their influence on circuit behavior.

4.1 Ideal Model

First, we shall analyze the SC Amplifier in ideal conditions – without offset voltage and capacitor mismatch. For this, in equations (1) – (12), we make V_{OS}=0, $C_{11}=C_{12}=C_1$, $C_{21}=C_{22}=C_2$ and respectively $C_{31}=C_{32}=C_3$. The resulting capacitor charges are replaced in the phase transition equations (16) – (19). The ideal equation system is given by eq. (25) – (28).

Subtracting equation (26) from (25) and respectively (28) from (27), we get

$$C_1 V_{Id} = C_2 V_{Od}(\Phi_2) \tag{20}$$

$$V_{Od}(\Phi_1) = V_{Od}(\Phi_2) \tag{21}$$

In the ideal case, the output voltage model is very simple: in both phases, the differential output voltage is equal to V_{Id} multiplied by the stage gain, C_1/C_2. We note that, if no offset is present, the output voltage is accurate during the *input sampling phase* as well.

$$V_{Od}(\Phi_2) = \frac{C_1}{C_2} V_{Id} \tag{22}$$

For deducing a model for V_X voltage, we sum (27) and (28) equations. We get:

$$V_X(\Phi_1) = V_{CM} \tag{23}$$

Finally, summing (25) and (26) equations, and using the fact that $V_X(\Phi_1)=V_{CM}$, we get the base amplifier input voltage corresponding to the second phase:

$$V_X(\Phi_2) = \frac{2C_1 V_{CM}}{C_1 + C_2} - \frac{C_1 V_{Icm}}{C_1 + C_2} + \frac{C_2 V_{Ocm}}{C_1 + C_2} \tag{24}$$

To this ideal model, we shall add the offset voltage and capacitor mismatch effects.

4.2 Offset Voltage Effect

We now must update the (25) – (28) equation system, by introducing the offset voltage contribution. We notice that the offset voltage has the same contribution to the C_{11} capacitor charge in both phases: the $V_{OS}/2$ appears with the same sign both in $Q_{11}(\Phi_1)$ and $Q_{11}(\Phi_2)$ relations [eq. (1) and (7)].

So the C_{11} charge variation, ΔQ_{11}, is independent of the offset voltage. A similar conclusion is valid also for C_{12}, C_{12} and C_{22} capacitors. As a conclusion equations (25) and (26) remain valid (as they are the explicit form for $\Delta Q_{11}= \Delta Q_{21}$ and $\Delta Q_{12}= \Delta Q_{22}$ and all of this terms are independent of offset voltage). This technique of eliminating the offset voltage influence is called "*correlated double sampling*". The offset voltage is sampled in both phases so the charge transfer is not influenced by the offset.

The offset voltage affects the C_{31} and C_{32} capacitors only during the *input sampling* phase and with opposite signs. [see eq. (3), (6), (9), (12)] So the voltage stored on these capacitors will be affected by the base amplifier offset voltage.

$$C_1\left(V_{Icm} + V_{Id} - V_X(\Phi_1) - V_{CM} + V_X(\Phi_2)\right) = C_2\left(V_X(\Phi_1) - V_{CM} - V_X(\Phi_2) + V_{Ocm} + V_{Od}(\Phi_2)\right) \tag{25}$$

$$C_1\left(V_{Icm} - V_{Id} - V_X(\Phi_1) - V_{CM} + V_X(\Phi_2)\right) = C_2\left(V_X(\Phi_1) - V_{CM} - V_X(\Phi_2) + V_{Ocm} - V_{Od}(\Phi_2)\right) \tag{26}$$

$$C_3\left(V_{Ocm} + V_{Od}(\Phi_1) - V_X(\Phi_1)\right) = C_3\left(V_{Ocm} + V_{Od}(\Phi_2) - V_{CM}\right) \tag{27}$$

$$C_3\left(V_{Ocm} - V_{Od}(\Phi_1) - V_X(\Phi_1)\right) = C_3\left(V_{Ocm} - V_{Od}(\Phi_2) - V_{CM}\right) \tag{28}$$

We use the same method of solving the system – we sum and subtract the equations two by two. Equations (25) and (26) are unchanged, due to the *correlated double sampling*. The offset voltage appears in both (27) and (28) equations, but with opposite signs, so it is canceled when summing.

As a result, the only change to the ideal model is that the output voltage is affected by the offset voltage during the *input sampling* phase.

$$V_{Od}(\Phi_1) = V_{Od}(\Phi_2) + V_{os}/2 \tag{29}$$

All other model equations are not affected by offset.

4.3 Capacitor Mismatch Effect

In this section, we shall develop a model for the output differential voltage, which includes capacitor mismatch effects.

Let us consider C_{11} and C_{12} matched capacitors. Both of them are designed to have the same nominal value, $C_{1,\mathrm{nom}}$. Due to process variations, the capacitors values result C_{11} and respectively C_{12}, different from the nominal value and also different one from the other. For this reason, we introduce the capacitor average value,

$$C_1 = (C_{11} + C_{12})/2 \tag{30}$$

and the capacitor mismatch

$$\Delta C_1 = (C_{11} - C_{12})/2 \tag{31}$$

While the nominal value, $C_{1,\mathrm{nom}}$, is a constant specified by design, the average value, C_1, varies randomly from one chip to another. Its mean value is equal to $C_{1,\mathrm{nom}}$ and the standard deviation is given by the process. The capacitor mismatch, ΔC_1 is also a random variable, with the mean value equal to 0. []

We notice that the output voltage is not affected by C_{31} and C_{32} capacitors exact values, so the mismatch between these two capacitors has no influence on output voltage accuracy.

Replacing the new capacitor values into (16) – (19), and applying the same solving method, (Danchiv, 2007) we get

$$V_{Od}(\Phi_2) = \frac{C_1}{C_2} V_{Id} + \frac{C_1}{C_1 + C_2}\left(\frac{\Delta C_1}{C_1} - \frac{\Delta C_2}{C_2}\right)(V_{Icm} - 2V_{CM} + V_{Ocm}) \tag{32}$$

and respectively

$$V_X(\Phi_2) = \frac{2C_1 V_{CM}}{C_1 + C_2} - \frac{C_1 V_{Icm}}{C_1 + C_2} + \frac{C_2 V_{Ocm}}{C_1 + C_2} - \frac{\Delta C_1}{C_1 + C_2} V_{id} + \frac{\Delta C_2}{C_1 + C_2} V_{od}(\Phi_2) \tag{33}$$

Equations (23) and (29) are unchanged, as they result from the C_{31}, C_{32} capacitor charge conservation.

4.4 Output Voltage Model

Bringing together the results form previous sections, we propose the following model for the output differential voltage and base amplifier input voltage:

$$V_{Od}(\Phi_2) = (C_1/C_2)V_{Id} + \frac{C_1}{C_1 + C_2}\left(\frac{\Delta C_1}{C_1} - \frac{\Delta C_2}{C_2}\right)(V_{Icm} - 2V_{CM} + V_{Ocm}) \tag{34}$$

$$V_{Od}(\Phi_1) = V_{Od}(\Phi_2) + V_{os}/2 \tag{35}$$

$$V_X(\Phi_1) = V_{CM} \tag{36}$$

$$V_X(\Phi_2) = \frac{2C_1 V_{CM}}{C_1 + C_2} - \frac{C_1 V_{Icm}}{C_1 + C_2} + \frac{C_2 V_{Ocm}}{C_1 + C_2} \tag{37}$$

Taking into account that the capacitor variation is usually very small and the precision needed in modeling V_X is not too high, we considered the ideal model [given by (24)] to be accurate enough.

5. PERFORMANCE EVALUATION

In this section, we shall use the previously deduced model to evaluate some SC amplifier parameters and determine the critical factors influencing them.

5.1 Differential Gain and Gain Accuracy

From the output voltage model [equation (34)], the differential to differential voltage gain is given by C_1/C_2. But C_1 represents the mean value of C_{11} and C_{12} while C_1 represents the mean value of C_{21} and C_{22} [see (30). In conclusion, the differential gain is given by:

$$A_{dd} = \frac{C_1}{C_2} = \frac{C_{11} + C_{12}}{C_{21} + C_{22}} \tag{38}$$

This result shows that the differential gain is not influenced by the C_{11} versus C_{12} and respectively C_{21} versus C_{22} capacitors matching, as is the case for the common mode rejection (see next section).

The matching strategies for optimizing gain accuracy and common mode rejection are different. To get a common mode rejection, C11 must be matched with C12 and C21 must be matched with C22. To get good gain accuracy, C11, C12 capacitor group must be matched with C21, C22 capacitor group.

5.2 Common Mode Rejection

We are interested in the common-mode input to differential output gain. The input common-mode voltage is centered on $2V_{CM}$-V_{Ocm} (V_{Od} is zero when the V_{Icm} is equal to $2V_{CM}$-V_{Ocm}). When the common-mode input differs from this central value, the difference is amplified by [see equation (34)]:

$$A_{cd} = \frac{V_{Od}}{V_i} = \frac{C_1}{C_1 + C_2}\left(\frac{\Delta C_1}{C_1} - \frac{\Delta C_2}{C_2}\right) \tag{39}$$

The common-mode gain, A_{cd}, is directly proportional to the relative capacitance mismatch. This result is intuitively explained by noting that the amplifier has two symmetrical but independent capacitive signal paths. An asymmetry between the two paths will result in a common mode signal propagating differently to the two outputs and will lead to an output differential signal. The common-mode rejection ratio results

$$CMRR = \frac{A_{dd}}{A_{cd}} = \frac{A_{dd} + 1}{(\Delta C_1 / C_1) - (\Delta C_2 / C_2)} \qquad (40)$$

This relation is useful only if ΔC_1 and ΔC_2 are known. However, technological mismatch is a random process so we can only know the capacitive mismatch standard deviation. For this reason, when evaluating (40), we should consider the capacitive mismatch square mean value. The minimum common mode rejection is then given by:

$$CMRR_{\min} = \frac{A_{dd} + 1}{\sqrt{(\Delta C_1^{\max} / C_1)^2 + (\Delta C_2^{\max} / C_2)^2}} \qquad (41)$$

where $\Delta C_{1,2}^{\max}$ are the maximum capacitive mismatches, for a certain degree of confidence.

We note that, for a fully differential amplifier, we can also define the differential input to common-mode output and respectively common-mode input to common-mode output gains, A_{dc} and A_{cc}. However, the output common-mode is controlled by a common-mode feedback block that is mainly responsible for these performances. Also, we note that equation (34) predicts the gain between V_{CM}, respectively V_o and differential output. However, the voltage variations on V_{CM} and V_o are generally small enough not to disturb the differential output voltage.

5.3 Input Common Mode Range

The input common mode range for the SC stage presented in Fig. 1 is limited by the base amplifier input common mode range. For the amplifier to function properly, we must assure that the base amplifier input, V_X does not exceed the allowed operation range.

During the *input sampling* phase, the base amplifier input voltage is $V_X(\Phi_1)=V_{CM}$, independent on the SC stage common mode, V_{Icm}. This result requires that V_{CM} is chosen inside the base amplifier input voltage range, but imposes no restrictions on V_{Icm}. During the *signal evaluation* phase, V_X is proportional to the input common mode [see eq. (37)]. Generally, the coefficient $C_1/(C_1+C_2)\approx 1$ so the SC stage will have practically the same common mode range as the base amplifier. We note that, even if we cannot substantially increase the SC stage common mode range (compared to the base amplifier input range), we can shift it by choosing appropriate V_{CM} and V_{Ocm} values.

6. SIMULATION RESULTS

In this section, the SPICE simulation results are presented and the compared with the manual model.

6.1 Transient Behaviour

The designed amplifier had a gain of 10 (C_1=5 pF, C_2=0.5 pF). The supply voltage is 5 V and both V_{CM} and V_{Ocm} where chosen equal to half supply. A base amplifier 10 mV offset was also introduced to highlight the correlated double sampling effect.

The SPICE simulated input and output differential voltages, V_{Id} and V_{Od}, are presented in Fig. 4. For a 20 mV differential input voltage, the differential output voltage settles around 200 mV.We notice that, at phase transition, the circuit has an exponential transient response before settling to a constant value. The exponential time constant is determined by the switch on resistance and by the capacitors values.Fig. 4 also shows that the final settling value is different between phases. During *signal evaluation* phase, the output settles with very good accuracy around 200 mV. During *input sampling* phase, the offset voltage is not compensated and the output settles about 10 mV lower. This result is in good agreement with the model [see eq. (34) and (35)].The base amplifier input common mode signal, V_X, is presented in Fig. 5. The V_X signal needs a transition phase, during which the capacitors are loaded. After the stable operation was achieved, V_X varies between V_{CM} (in *input sampling* phase) and the value predicted by equation (37) (*signal evaluation* phase).

6.2 Common Mode Rejection

In order to check the common mode gain [predicted by eq. (39)], we introduced an "artificial" unbalance between matched capacitances and measured the SC amplifier output differential signal for V_{Id}=0. We used V_{Icm} = 0 V and V_{CM}=V_{Ocm}=2.5 V. This corresponds to an actual "input common mode signal" of $V_{Icm}-2V_{CM}+V_{Ocm}= -2.5$ V.

The simulated differential output voltage values for capacitances mismatch between 0.1 and 5 % are presented in Table 1 and compared to the manual model estimated results.

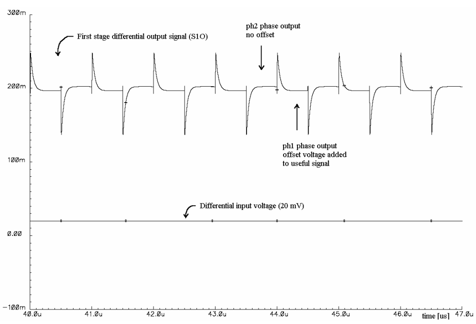

Fig. 4. SC Amplifier input and output signals.

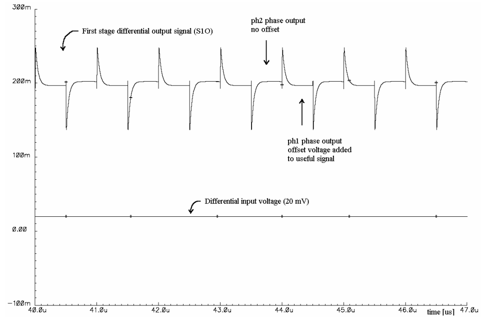

Fig. 5. Base amplifier input signal.

Simulation results predict a small common mode gain even for perfectly matched capacitors, but the mismatch influence becomes dominant even at 0.1 % mismatch. The manual estimation results differ from simulation results with less then 5 %. We also notice that $\Delta C_1/C_1$ and $\Delta C_2/C_2$ mismatches have similar effects on the output voltage. The common mode rejection, predicted by (40), is given in Table 2 for to different capacitive mismatches. We considered similar mismatches for both capacitor ratios. We also checked the V_{Od} variation over the input common mode range, at a fixed capacitor mismatch. Results are given in Table 3.

Table 1

C_1	V_{Od} sim	V_{Od} calc	C_2	V_{Od} sim	V_{Od} calc
[%]	[mV]	[mV]	[%]	[mV]	[mV]
0	-0.08	0.0	0	-0.08	0.0
0.1	-4.67	-4.5	0.1	4.46	4.55
0.5	-23.0	-22.7	0.5	22.6	22.7
1	-45.8	-45.5	1	45.3	45.4
5	-229	-227	5	227	227

6.3 Input Common Mode Range

As discussed in the previous section, the SC stage input common mode range is determined by three main factors: base amplifier common mode range, output common mode voltage, V_{Ocm} and internal common mode voltage, V_{CM}. The SC amplifier gain has also an influence, but relatively small. We choose the output common mode voltage to be half supply, V_{Ocm}=2.5 V, to facilitate the interface to the next stage and to allow maximum output differential swing. In order to have the input common mode centered, the internal common mode voltage also results V_{CM}=2.5 V.

Table 2

ΔC/C [%]		0.1	0.5	1	5
CMRR [db]	sim	77.8	63.8	57.8	43.8
	calc	74.5	60.7	54.7	40.7

Table 3

V_{Icm} [V]		0	1	2.5	4	5
V_{Ocm} [mV]	sim	-45.8	-27.5	-0.1	27.4	45.6
	calc	-45.4	-27.2	0.0	27.27	45.4

In the conditions mentioned above, we have swept the input common mode voltage from rail to rail. The resulting V_X voltages are presented in **Error! Reference source not found.**. The simulation results show very good agreement with the values predicted by equation (37). We note that a rail to rail base amplifier was needed for this evaluation.

Table 4

V_{Icm}	$V_X(\Phi_1)$ sim.	$V_X(\Phi_1)$ calc.	$V_X(\Phi_2)$ sim.	$V_X(\Phi_2)$ calc.
[V]	[V]	[V]	[V]	[V]
0	2.49	2.5	4.76	4.77
1	2.50	2.5	3.86	3.86
2	2.50	2.5	2.95	2.95
3	2.50	2.5	2.05	2.04
4	2.50	2.5	1.14	1.14
5	2.51	2.5	0.24	0.23

7. CONCLUSIONS

Many high performance, discrete time, amplifiers rely on the SC technique, as it provides offset cancellation and accurate gain at reasonable speed and area consumption. This paper presents a simple analytical d.c. model, for a standard topology switched capacitor amplifier. The output voltage and base amplifier input voltage are determined. The model takes into account the base amplifier offset voltage; highlighting offset cancellation (correlated double sampling). The capacitor mismatch is also considered, making this model well suited for analyzing the common mode rejection. The SC amplifier common mode input range is analyzed. The presented amplifier had a gain of 10 and was designed in a 0.6 µm technology. The simulated common mode gain and common mode rejection are in good agreement with the ones estimated by manual analysis.

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