Interface with Simultaneous Sampling of Analog Inputs for Power Quality Measurement: Testing Programs and Experimental Results

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Abstract: The waveforms and values of monitored analog inputs are modified and the instantaneous values are important for the after-failure analysis and diagnosis when an event (fault, disturbance) appears in energetic systems. Several programmable electronic modules for power quality measurement and monitoring different specific transient events in power systems require an interface with synchronized sampling of all analog inputs and with high and settable sampling rate. The paper deals with some design aspects and characteristics of such interface entirely controlled by PC104 CPU and some software applications for testing its operation and an analysis of results obtained using this interface for data acquisition in energetic system. The programs were implemented using C programming language.

Keywords: Data acquisition, Interface, Sampling, Analog inputs, Current, Voltage, Programs, Flowcharts, Equipment, Events.

1. INTRODUCTION

A definition of power quality is given in various sources, e.g. Bollen and Gu (2006), Bollen (2000), Fuchs and Masoum (2008), Baggini (2008), Kusko and Thompson (2007), Lee et. al. (2004). Any deviation of voltage or current from the ideal is a power quality disturbance. Methods for classification or recognition of power quality disturbances are presented in Lee and Dash (2003), Dash et. al. (2003), Santoso et. al. (200a,b).

No real-life power source is ideal and generally can deviate in at least the following ways:

- variations in the peak or RMS (root-mean-square) voltage;
- abrupt, very brief increases in voltage;
- the nominal voltage drops below 90% for more than 1 minute;
- the nominal voltage rises above 110% for more than 1 minute;
- variations in the frequency;
- variations in the wave shape (usually described as "harmonics").

More than 50% of power quality problems are generated by natural and unpredictable events. There are three main sources of poor power quality related to utilities, presented in Fuchs and Masoum (2008): the point of supply generation, the transmission system, and the distribution system. Causes of disturbances in power systems, power quality improvement techniques and classification of power quality events are also given in Fuchs and Masoum (2008).

The measures used for estimate the power quality are presented in Fuchs and Masoum (2008), Baggini (2008); they are the following: harmonics, the average value of non-sinusoidal waveform, the RMS value of non-sinusoidal waveform, form factor, ripple factor, harmonic factor, total harmonic distortion etc. A system for detection and classification of voltage disturbances is presented in Matz et. al. (2007). This system applies the following methods to detect and classify the power quality disturbances: digital filtering and mathematical morphology are used to detect and classify transients and waveform distortions, while in case of short and long duration disturbances (such as sags, swells and interruptions) the analysis of the RMS value of the voltage is employed. New architectures for modern electrical systems have been developed, and novel active filtering techniques and devices have been proposed, which will be able to change the power factor and to eliminate undesired harmonics in Qun Zhao Lee and Fu Sheng, T. (2002), Bor Ren and Chun Hao (2004). A very flexible AC/DC converter featuring high-output current, reduced voltage ripple and highly adjustable current control is described in Muzi and Passacantando (2008).

Many equipments and instruments for power quality measurement, monitoring and diagnosis of energetic systems were designed and implemented in the last years (Pancu et. al., 2009 ; Purcaru I. et. al., 1998 ; Grigorescu et. al., 2010 ; Iordache et. al., 1996; Kilter et. al., 2009;

Nicolae et. al., 2011; Purcaru D. et. al. (2010a); Ferrero 2002, Purcaru D. and Purcaru A., 2013). The researchers propose various methods for measurement of power quality parameters in Pardeshi (2007), Petrovic (2007), Purcaru et. al. (2008). Monitoring and diagnosis procedures and equipments recommended for energetic systems are presented in Brahma (2005), Muzi and Passacantando (2007). A distributed data acquisition system with functional nodes based on PC/104 compatible modules is proposed in Purcaru I. and Purcaru D. (2010c).

Several programmable electronic modules for data acquisition (placed into different locations, near the input signals provided by the observed process) are presented in Purcaru I. and Purcaru D. (2010c), Purcaru D. et. al. (2010a,b), Purcaru I. et. al. (1998). Some of these equipments require a multifunctional and low cost interface with synchronized sampling of all analog inputs and with high and settable sampling rate. This interface is also useful in other high speed data acquisition systems. An interface with these characteristics is presented in Purcaru D. et. al. (2010b) and the applied method for synchronized sampling of analog inputs is detailed in Purcaru D. and Purcaru A. (2011), as a PC104 interface; an application can be given in Purcaru D. and Purcaru A. (2013).

The main purpose of this paper is to present some testing programs for the PC104 interface with synchronized sampling of analog inputs and some experimental results.

2. DESIGN ASPECTS AND CHARACTERISTICS OF THE PC104 INTERFACE WITH SYNCHRONIZED SAMPLING OF ANALOG INPUTS

The block diagram of the PC 104 interface with synchronized sampling of analog inputs is shown in Fig. 1 and the hardware solution is detailed in Purcaru et. al. (2010b). The main blocks of this interface are the octal bus transceiver, address decoder, programmable peripheral interface, programmable interval timer and analog-to-digital conversion module. Their functions are presented in Purcaru D. et. al. (2010b). The principle of synchronized sampling of analog inputs is presented in Purcaru D. and Purcaru A. (2011).

The hardware achitecture of the analog-to-digital conversion module with synchronized sampling of all analog inputs is presented in Fig. 1 and its operating sequence is shown in Fig. 2.

The 16-bit analog-to-digital converter LTC1864 includes the sample-and-hold circuit, has a differential analog input and a serial output (SDO). It is directly connected to signal source as a consequence to its high impedance of analog input. The conversion cycle begins on the rising edge of CONV and the converter output (SDO) is in high-impedance state (Hi-Z) during the high level of CONV. The last output (PC7) of PORT C of the programmable peripheral interface provides the CONV signal. The serial output (SDO) of each LTC1864 circuit is enabled on the falling edge of CONV, and SCK synchronizes the data transfer with each bit (B15, B14,…, B0) being transmitted from SDO (on the falling edge of SCK), only after the falling edge of CONV.

The functional description of the octal D-type transparent latches (74HCT573) shows that

- the latches are transparent when LE= $\overline{SCK}$ is HIGH,
- the latches store the information when LE= $\overline{SCK}$ is LOW,
- the content of the 8 latches is available at the $Q_0,\dots,Q_7$ outputs when $\overline{OE}$ is LOW,
- the $Q_0,\dots,Q_7$ outputs go to the high-impedance OFF-state when $\overline{OE}$ is HIGH.

Three logic gates (Fig. 1) implement a combinational logic circuit which provides the control signals SCK (for all LTC1864 converters), LE and $\overline{OE}$ (for 74HCT573).

Fig. 2 shows the waveforms of CONV, SCK, LE and $\overline{OE}$, the serial output (SDO) only for one analog-to-digital converter (ADC 7 from Fig. 1) and only the Q7 output of 74HCT573 (D7 being the corresponding data input). The falling edge of SCK commands both the high level of LE (after the t_2 delay time) and SDO=B15 (after the t_3 delay time); B15 is MSB. Each bit (B15, B14,…, B0) is available at the corresponding 74HCT573 output after the t_4 delay time (Fig. 2). The PC104 processor reads the 74HCT573 outputs (Q7, Q6, … , Q0) on the rising edge of SCK. Therefore, the processor reads the Bi bit ($i=0\div15$) of each LTC1864 serial output after the t_5 delay time (Fig. 2).

The conversion result after one "conversion – reading" cycle will be stored in 16 memory bytes of the PC104 compatible UC, at successive addresses. We can consider a memory area of 16 rows and 8 columns which stores the analog-to-digital conversion results. By reading the memory columns we build the binary words corresponding to 8 analog inputs (Purcaru D. and Purcaru A., 2013).

The PC 104 interface with synchronized sampling of analog inputs is entirely controlled by PC104 CPU, and the programmable peripheral interface and the programmable interval timer can be programmed according to the desired application. The main characteristics of this interface are the following:

- 8 common-mode or differential analog inputs;
- 0-4V value domain of each analog input;
- all inputs are simultaneously sampled;
- high sampling rate (it can be over 100kS/s);
- settable sampling rate (the PC7 output of the programmable peripheral interface is used to start the analog-to-digital conversion);
- 16-bit resolution of the analog-to-digital conversion;
- 23 digital inputs/outputs, TTL compatible;
- PC104 bus compatibility;
- mechanical compatibility with PC104.

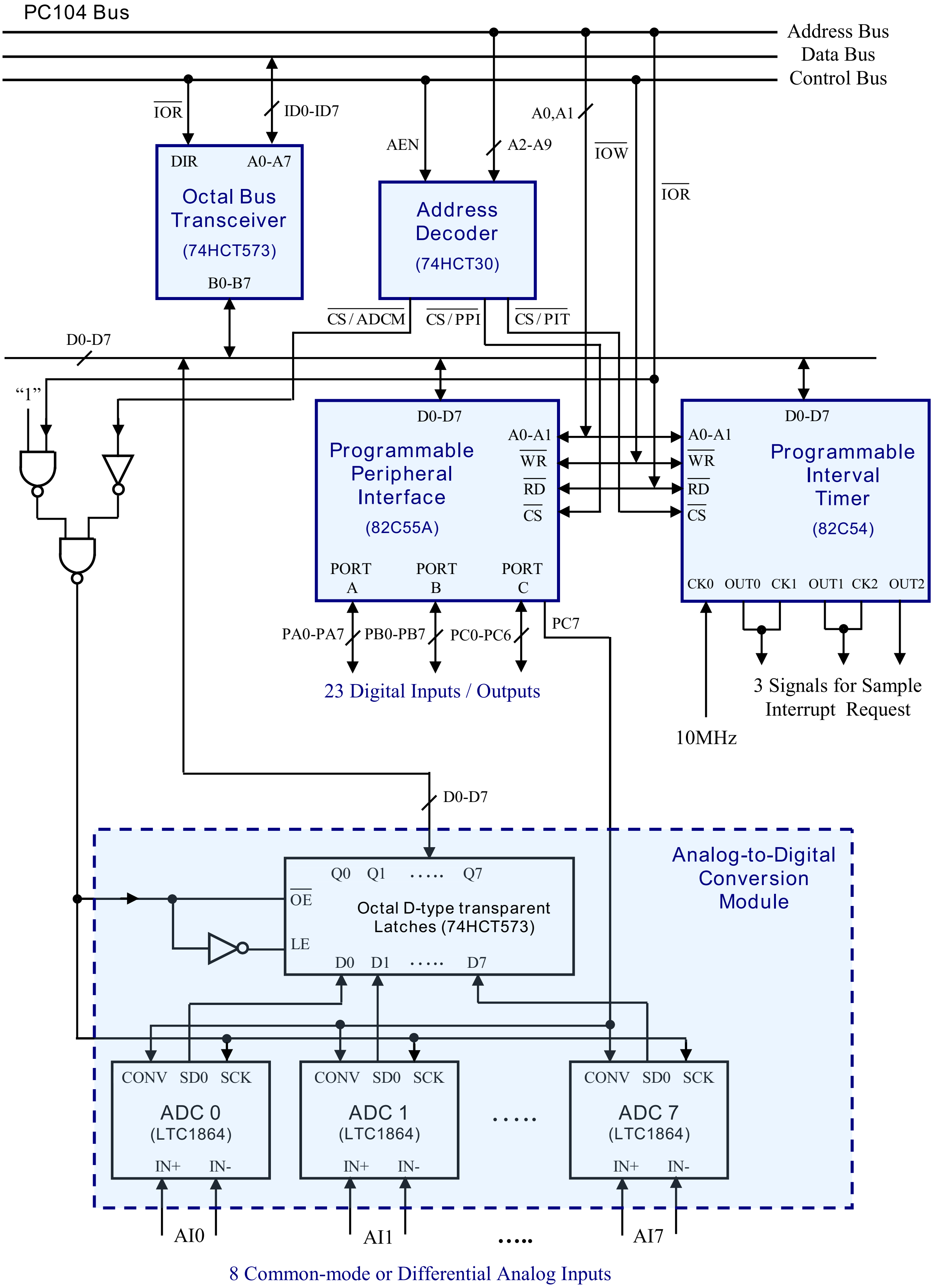

Fig. 1. Block diagram of the PC 104 interface with synchronized sampling of analog inputs.

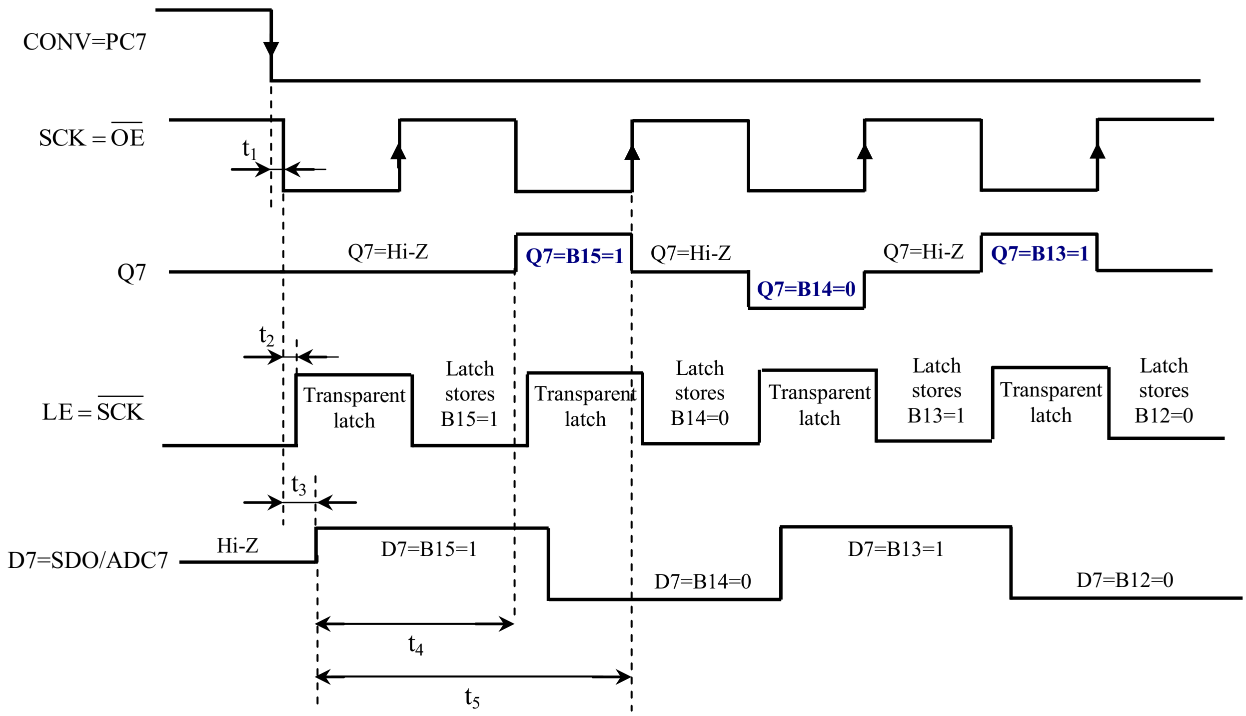

Fig. 2. Analog-to-digital conversion module – Operating sequence.

3. TESTING PROGRAMS

The PC104 interface with synchronized sampling of analog inputs is associated with two test applications which were implemented using C programming language (Schildt, 2003).

3.1 First Testing Program

The *ADC_AVG* software application is specific to PC104 interface with synchronized sampling of analog inputs and it runs during functional testing of the interface's analog-to-digital converter.

The application follows 3 main running steps:

- acquires 10 successive samples from each of the 8 input analog channels;
- displays acquired values, as intermediate;
- displays the 10-sample average value for each of the 8 input analog channels.

The application functionality is revealed through the logical diagram from Fig. 3.

The application program features conversion function *conv_8chn()* that handles the built of an 8 channel conversion values array, later displayed as a collection of intermediate values.

Each acquisition is simultaneously started for all channels. The acquisition latches an 8-bit word, which contains the bits of successive ranks, for each of the 8 acquisition values. Each conversion value is stored in a 16-bit word. The conversion algorithm is graphically presented in Fig. 4.

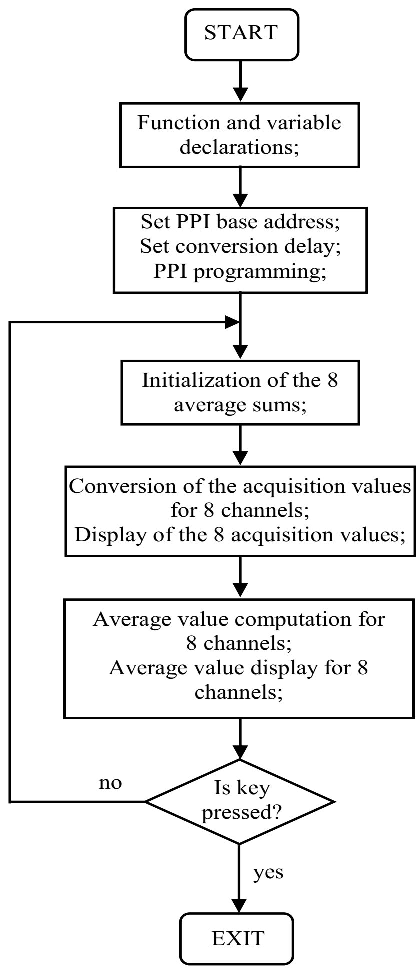

Fig. 3. *ADC_AVG* functioning diagram

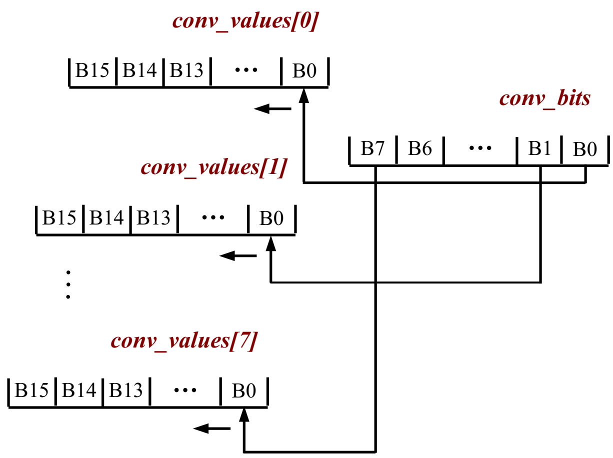

Fig. 4. *conv_8chn()* conversion principle

According to the algorithm, the function has the implementation principles of the logical diagram from Fig. 5.

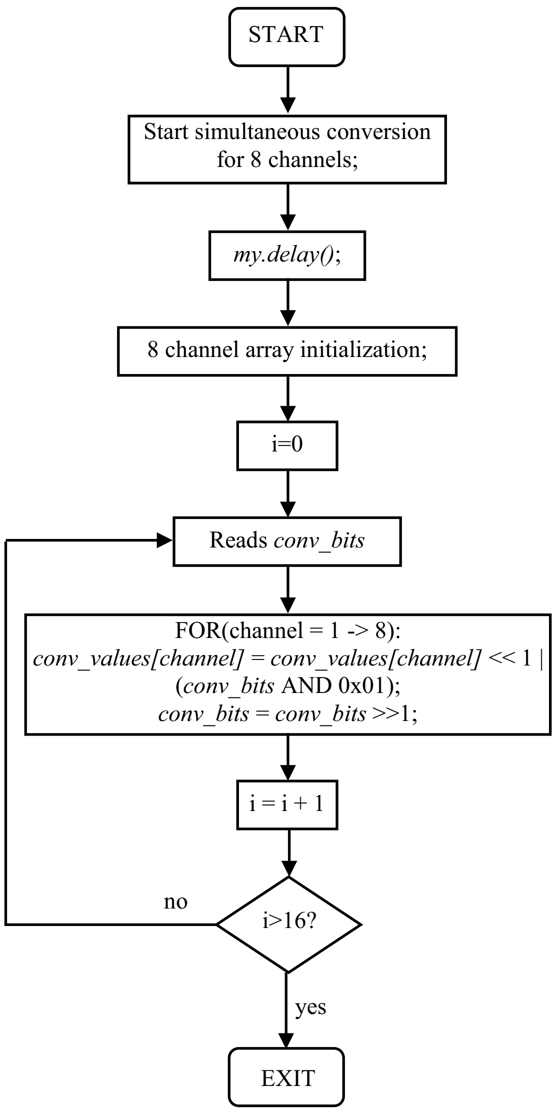

Fig. 5. *conv_8chn()* functioning diagram

The acquisition impulse length and duration are establish through timing function *my_delay(unsigned long delay)*.

The program source code with in-line comments is listed below.

```
#include <dos.h>
#include <conio.h>
#include<stdio.h>

//establishing interface base address
#define PORT_ADC 0x300

//addressing PPI ports
#define PORTA 0x308
#define PORTB 0x309
#define PORTC 0x30A

//addressing PPI control port
#define CONTROL_PORT 0x30B
//programming PPI with control word
#define CONTROL_WORD 0x80

//variable declaration

//my_delay temporisation:
unsigned long tempor;
unsigned int portA_BA = 0x00;//base address
char text_portA_BA[100];
char ch; //for loop stop
//conversion bit storing array:
unsigned char conv_bits;
//conversion values storing  array:
unsigned int conv_values[10];
//binary display mask
unsigned char bin_mask;
//acquisition average array:
unsigned long avg[15];
//intermediate sums array:
unsigned long sum[15];

//function declarations and implementation
// temporization function:
void my_delay(unsigned long delay)
{
  while(delay > 0) delay --;
}

//conversion function for 8 synchronized
//input channels:
void conv_8chn()
{
  outportb(PORTC,0x80);//conv. start
  //ADconv. start impulse duration:
  my_delay(tempor);
  //reset start conversion bit:
  outportb(PORTC, 0x00);
//covering temporization until end //of AD
//conversion:
  my_delay(tempor);
//conversion values array //initialization
//(conv_values):
  for(int channel=0;channel < 8;channel++)
  {
    conv_values[channel] = 0x00;
  }

//collecting conversion result bits and
//decoding values (16-bit words):
  for (int i = 0; i<16; i++)
  {
    conv_bits = inportb(PORT_ADC);
    my_delay(100);
    for(int channel = 0; channel < 8; channel++)
    {
      conv_values[channel] =
```

```
       (conv_values[channel] << 1) |
      ((unsigned int)conv_bits & 0x01);
       conv_bits = conv_bits >> 1;
      }
   }
}

int main()
{
  printf("\nSet ADC base address:");
  scanf("%x", &portA_BA);
  //printf("\n%x", portA_BA);

  printf("\nSet temporization for one AD
conversion:");
  scanf("%ld",&tempor);

  //PPI programing
  outp(CONTROL_PORT, CONTROL_WORD);

  //initializare PORTC
  outportb(PORTC, 0x00);

//10-sample acquisition loop, synchronized for 8
//input channels ;
//displaying 10-sample average value for each
channel
  do
  {
  //init sum
    for(int i = 0; i<8; i++)
      sum[i] = 0;
  //displaying intermediate values
    for(i = 0; i <10; i++)
    {
      conv_8chn();
      for(int j = 0; j<8; j++)
      {
       printf("%4x ", conv_values[j]);
        sum[j] += conv_values[j];
      }
      printf("\n");
    }
  printf("\n");
//calculating and displaying average value for
each //channel
    for(i = 0; i<8; i++)
    {
      avg[i] = sum[i]/10;
      printf("%4x ", avg[i]);
    }
    printf("\n");
    getch();
  } while (!kbhit());
  return 1;
}
```

3.2 Second Testing Program

The software module *ADC_CONV* performs data acquisition and decoding of final values, for each of the 8 acquisition channels. This test application has the feature of signal viewing while the PC104 interface with synchronized sampling of analog inputs is in function, after easily synchronizing to an oscilloscope.

The application program has an initialization sequence and a main loop of acquisition/conversion/display. The initialization sequence sets the base address for A-D converter, sets the conversion temporization for additional function *my_delay(unsigned long delay)* and programs the PPI unit for storing the conversion bits. Meanwhile, the loop follows the steps of sending the command, storing, acquiring and converting the values for each of the 8 analog input channels.

The test application has the functional diagram from Fig. 6 .

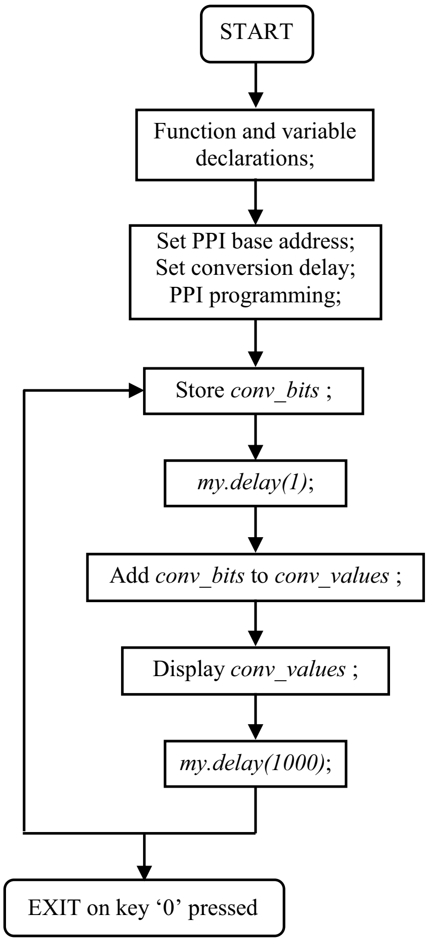

Fig. 6. *ADC_CONV* functioning diagram

The source code for the application program is the following:

```
#include <dos.h>
#include <conio.h>
#include<stdio.h>

#define PORT_ADC 0x300

#define PORTA 0x308
#define PORTB 0x309
#define PORTC 0x30A

#define CONTROL_PORT 0x30B
#define CONTROL_WORD 0x80

unsigned long tempor;//temporizare my_delay
unsigned int portA_BA = 0x00;//base address
char text_portA_BA[100];
char ch; //exit program character
unsigned  char  conv_bits;//storing  conversion
bits
int conv_values[10];//conversion values array
//temporization function
void my_delay(unsigned long delay)
{
  while(delay > 0) delay --;
}
```

```
int main()
{
//initializations
  printf("\nSet base address for ADC:");
  scanf("%x", &portA_BA);
  printf("\nSet conversion delay");
  scanf("%ld",&tempor);
  outp(CONTROL_PORT, CONTROL_WORD);

//PORTC initialization
  outportb(PORTC, 0x00);
//analog channel conversion loop
  do
  {
    //start conv and delay
    outportb(PORTC,0x80);
    my_delay(tempor);
    outportb(PORTC, 0x00);
    my_delay(tempor);
    //init conv_values
    for(int channel = 0; channel < 8; channel++)
    {
      conv_values[channel] = 0x00;
    }
  //preluare biti
    for (int i = 0; i<16; i++)
    {
      conv_bits = inportb(PORT_ADC);
      my_delay(1);
      for(int   channel   =   0;   channel   <   8;
channel++)
      {
        conv_values[channel] =
      (conv_values[channel] << 1) |
               ((unsigned int)conv_bits & 0x01);
        conv_bits = conv_bits >> 1;
      }
    }
//displaying conversion values
    long delay_count;
    for(int count = 0; count < 8; count++)
    {
      printf("   %x ", conv_values[count]);
    }
    printf("\n");
for(delay_count=0;delay_count<10000;delay_count+
+)
    {
      my_delay(1000);
    }
    if (ch == '0')
         break;//program   exits   at   key   ‘0’
pressed
  }while(!kbhit());
  return 1;
}
```

4. EXPERIMENTAL RESULTS

Many programmable electronic modules for power quality measurement or monitoring and recording different specific transient events (Iordache S. et. al., 1996), Purcaru I. et. al. (1998), Purcaru D. et. al. (2010a)) are very much of use in substations and hydroelectric power stations in Romania. These electronic equipments perform analog and digital signal acquisition and some of them already contain a PC104 interface with synchronized sampling of analog inputs. For example, the disturbance monitoring device PC-08/104 performs the synchronized sampling of eight analog inputs: URo – voltage of the R phase, USo – voltage of the S phase, UTo – voltage of the T phase, Uh – homopolar voltage, IRo – current of the R phase, ISo – current of the S phase, ITo – current of the T phase, Uex – excitation voltage for a hydrogenerator.

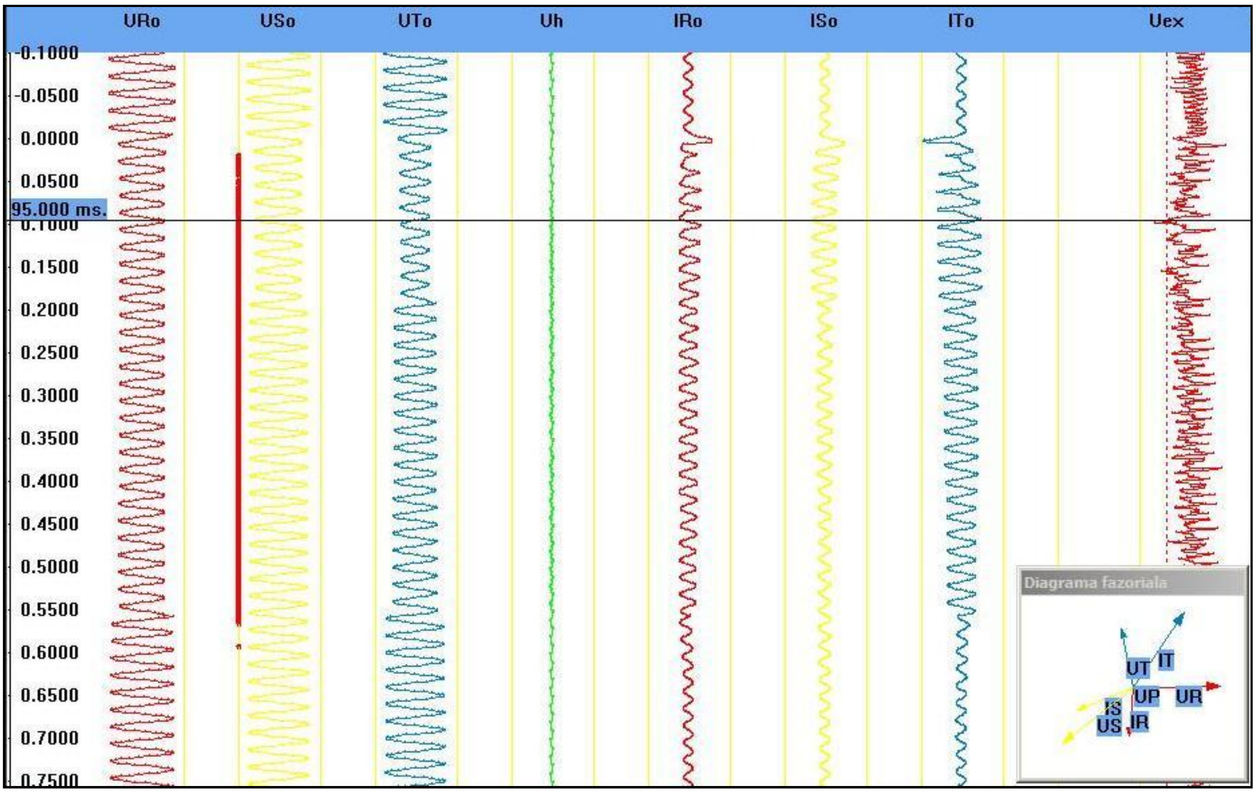

Fig. 7. The waveforms of the analog inputs (URo, USo, UTo, Uh, IRo, ISo, ITo, Uex) before, during and after an event supervised using PC-08/104.

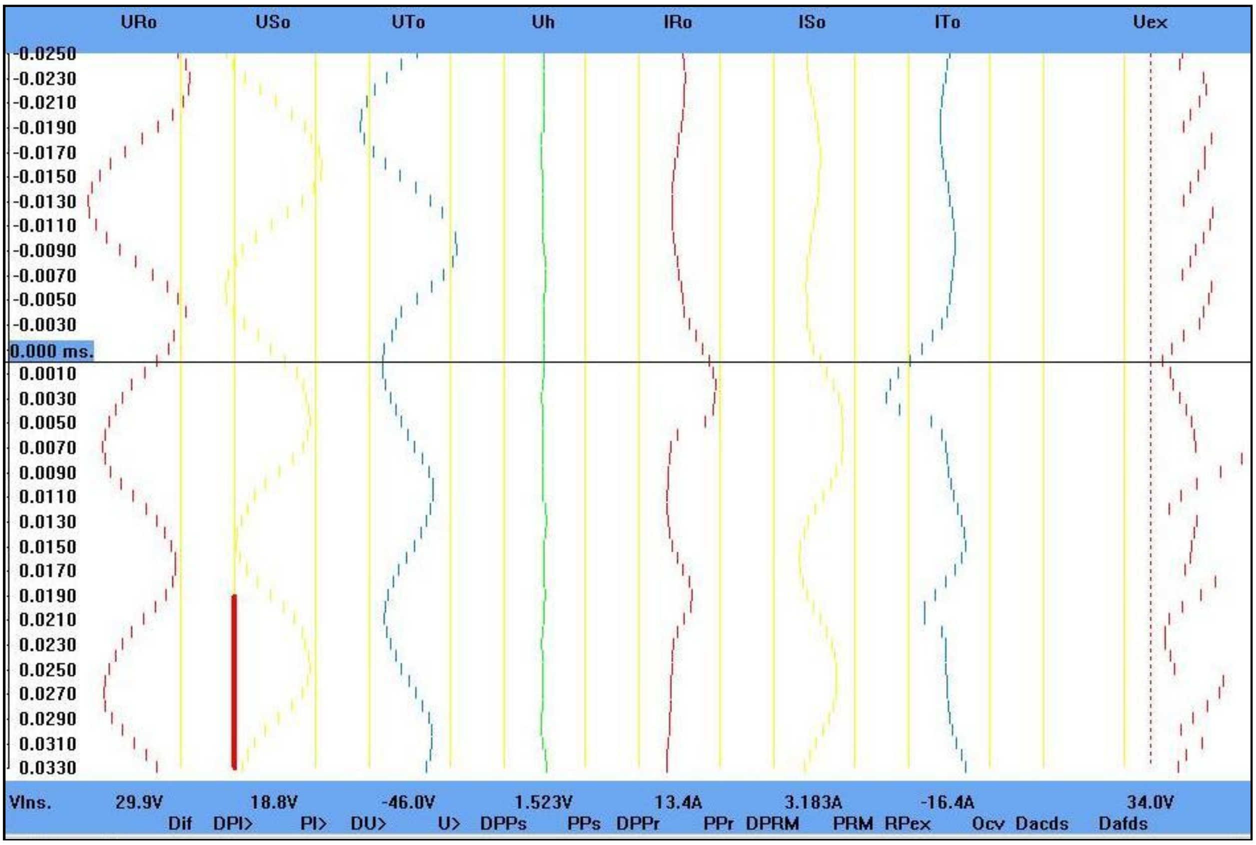

Fig. 8. The acquired samples of all analog inputs between the moments t_1= - 0.0250s and t_2= 0.0330s.

Moment(ms)	USo(V)	Uex(V)	ITo(A)	ISo(A)	IRo(A)	Uh(V)	URo(V)	UTo(V)
-10.000	-30.2V	141.8V	2.896A	-0.95A	-2.07A	-2.00V	-55.6V	84.2V
-9.000	-52.3V	120.0V	3.045A	-1.69A	-1.33A	0.165V	-32.1V	86.3V
-8.000	-65.1V	105.3V	2.698A	-2.34A	-0.26A	4.046V	-4.92V	78.3V
-7.000	-77.4V	87.4V	2.252A	-2.63A	0.515A	4.046V	22.6V	62.8V
-6.000	-82.8V	161.9V	1.559A	-2.98A	1.383A	2.785V	47.4V	40.5V
-5.000	-80.2V	155.5V	0.668A	-2.68A	2.002A	1.814V	66.5V	14.4V
-4.000	-67.8V	141.5V	-0.32A	-2.34A	2.448A	1.038V	79.5V	-13.3V
-3.000	-49.4V	129.9V	-2.50A	-2.34A	5.048A	0.941V	70.2V	-23.0V
-2.000	-26.3V	90.2V	-6.46A	-1.20A	7.690A	2.105V	60.0V	-30.6V
-1.000	-6.20V	59.9V	-11.1A	0.560A	10.8A	2.105V	50.5V	-43.9V
0.000	18.8V	34.0V	-16.4A	3.183A	13.4A	1.523V	29.9V	-46.0V
1.000	39.3V	56.6V	-21.2A	5.948A	15.3A	0.941V	9.001V	-46.2V
2.000	51.1V	62.4V	-24.8A	8.810A	16.1A	-0.94V	-12.9V	-40.3V
3.000	55.9V	79.1V	-26.6A	11.0A	15.8A	-2.78V	-28.6V	-31.4V
4.000	59.9V	94.9V	-20.8A	12.2A	15.4A	-1.81V	-39.3V	-23.6V
5.000	62.2V	109.1V	-7.05A	12.7A	11.7A	-1.32V	-50.2V	-13.5V
6.000	57.8V	118.0V	-2.84A	12.9A	-0.36A	-0.94V	-57.0V	-1.08V
7.000	50.3V	121.6V	-0.91A	12.6A	-3.26A	-0.94V	-61.1V	11.6V
8.000	32.7V	239.6V	-0.12A	12.0A	-3.91A	-1.71V	-58.1V	25.7V
9.000	10.1V	184.4V	0.520A	10.2A	-4.05A	-2.10V	-47.8V	35.7V
10.000	-13.9V	123.5V	1.262A	7.426A	-4.28A	-2.10V	-30.8V	42.9V

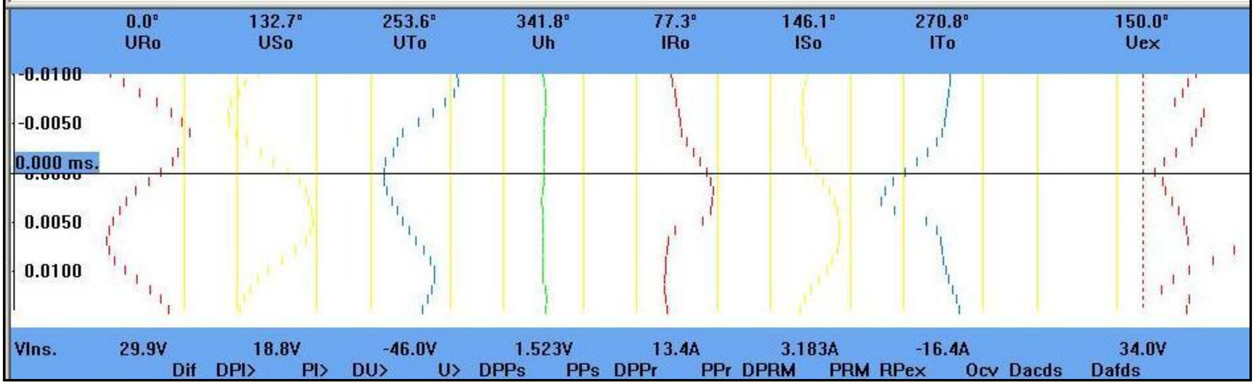

Fig. 9. The instantaneous values of eight analog inputs and the acquired samples between the moments t_1= - 10.000ms and t_2=10.000ms.

When an event (fault, disturbance) appears, the waveforms and values of these analog inputs are modified. The PC-08/104 device performs data acquisition, data temporary storage and data communication with an IBM-PC/AT compatible computer.

The waveforms of the analog inputs (URo, USo, UTo, Uh, IRo, ISo, ITo, Uex) before, during and after a real event supervised using PC-08/104 are presented in Fig. 7.

The time scale (in seconds) appears on the left side of the figure. The time origin (t=0.0000s) points to the start of the event; t<0 for the moments before the event (the preliminary-defect zone), and t>0 for the moments during and after the event. The cursor position is t=95.000ms and represents the measurement moment, selected by the user and marked with one horizontal line in figure. The vectorial diagram of the currents and voltages for the R, S, T phases at the measurement moment (during the event) are depicted on the bottom of Fig. 7, on the right side.

The waveforms of the analog inputs are obtained based on the samples acquired, shown in Fig. 8 between the moments t_1= - 0.0250s and t_2=0.0330s. The sampling rate is 1ms and all analog inputs are simultaneously sampled using the PC104 interface with synchronized sampling of analog inputs. The instantaneous values of each analog input at the moment t=0.000ms (selected with the cursor) are specified on the bottom of the figure ("VIns" row), below the corresponding waveform. The event (fault, disturbance) starts at this moment.

A table with the values of all samples acquired between two selected moments for all analog inputs simultaneously sampled with 1ms sampling rate can be displayed in the same figure with the waveforms. For example, the selected period is between t_1= - 10.000ms and t_2=10.000ms in Fig. 9. Twenty-one values for each analog inputs are displayed and the corresponding samples are marked on the waveform.

With one or many PC-08/104 equipments and one computer, various electronic structures can be configured for acquisition, monitoring and analysis of different events (faults, disturbances) specific to the energetic systems.

6. CONCLUSIONS

Several electronic equipments for power quality measurement or monitoring and recording different specific transient events from energetic systems contain a PC104 interface with synchronized sampling of analog inputs. Such equipments are very much of use in substations and hydroelectric power stations. This interface has a high and settable sampling rate and it is also useful in other high speed data acquisition systems.

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